

# **Photodiodes in Deep Submicron CMOS Process for Fully Integrated Optical Receivers**

Waqas Ahmad, Markus Törmänen  
and Henrik Sjöland

Department of Electrical and Information  
Technology (EIT), Lund University, Lund, Sweden

# Outline

- Motivation
- Introduction
- Design
- Measurements
- Equalization of CMOS photodiodes
- Conclusion

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# Motivation

- Low-cost short-haul optical communication
- MMF vs SMF
- Low cost VCSELS at 850nm wavelength
- Low-cost optical transceivers?
  - Use standard CMOS technology
- CMOS PDs have low responsivity and small BW
  - Very high penetration depth ( $d=18\mu\text{m}$ )
  - Shallow junctions

# Motivation

- Technology scaling is CMOS?

Process	Responsivity(A/W)	Bandwidth (MHz)
180nm	0.378	~5
130nm	0.300	~5
90nm	0.233	~5
65nm*	0.03	2.5

\* n+/p-sub photodiode

# Outline

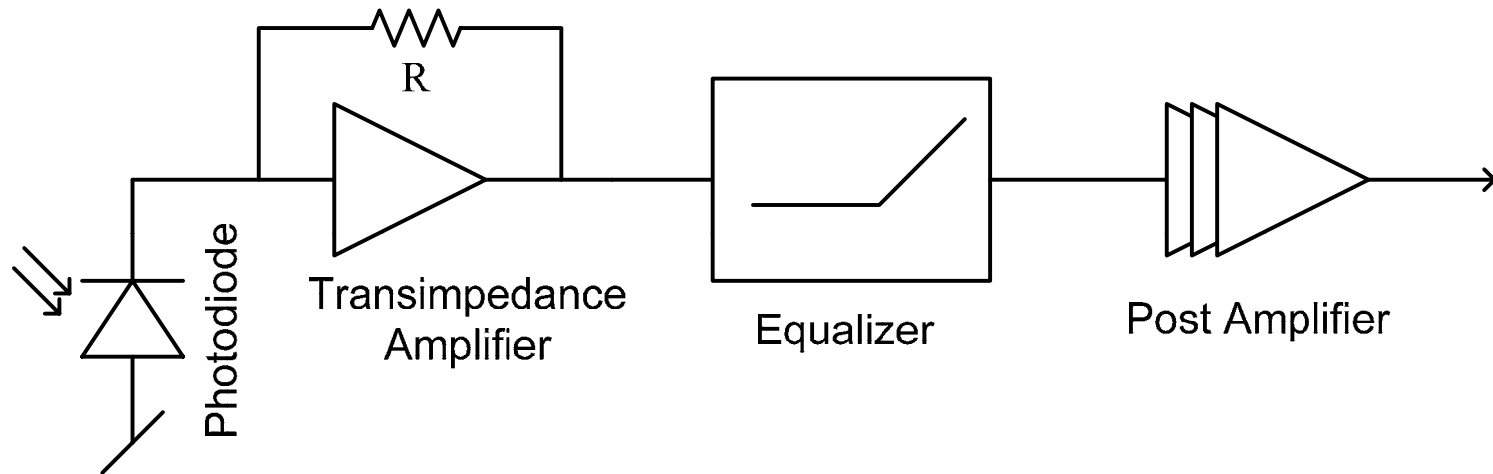
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# Introduction

- High speed optical receivers with CMOS PDs
  - Differential or Spatially Modulated PDs
  - Avalanche Photodiodes (APDs)
  - Equalization (Analog, Digital)

# Introduction

- A typical equalized optical receiver



- Freq. response of PD is required
- Modeling of CMOS photodiodes?
- Analog equalizer for integrated optical receiver



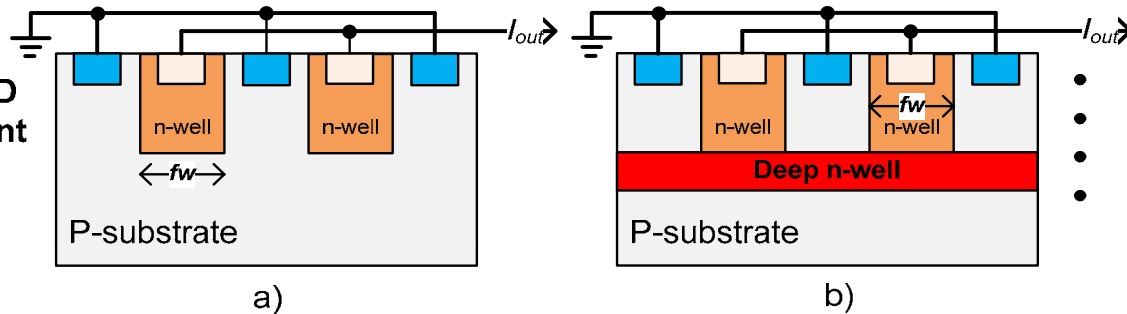
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# Design

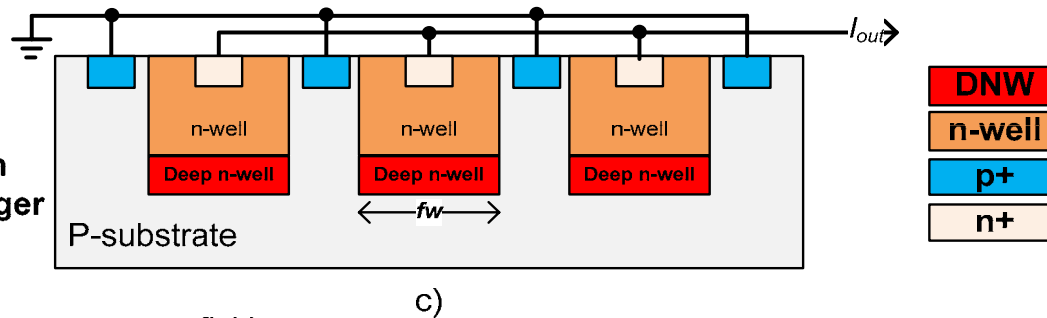
## • Cross section of the fabricated PDs

- Classical n-well/p-sub PD
- Two version with different number of fingers
- 17/29 finger PDs

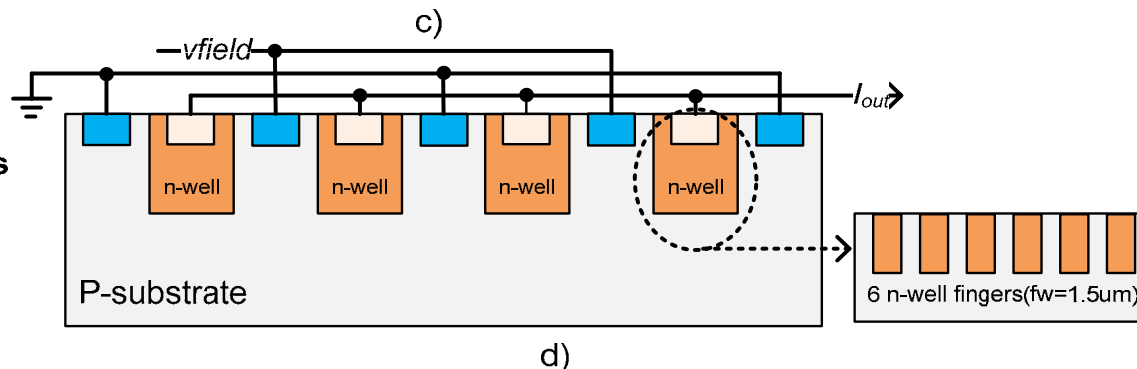


- DNW is used
- 24 n-well fingers
- More junctions
- Increased junction capacitance

- DNW is used as an extension to n-well
- Increased junction depth
- 9 fingers where each finger is 6μm wide

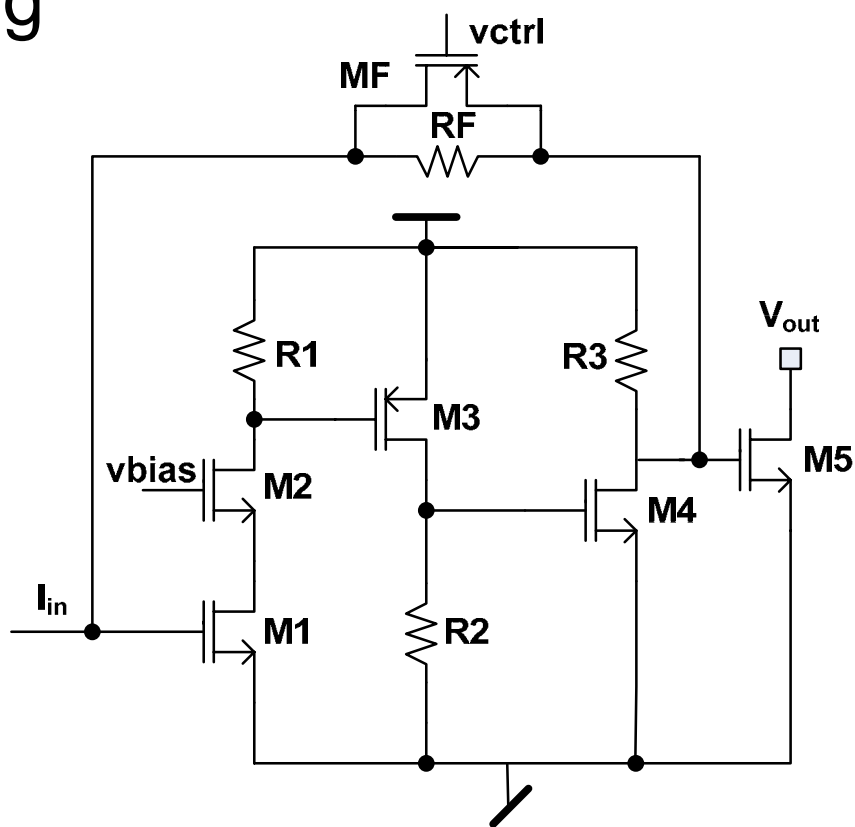


- External electric field is used to accelerate the slow carriers



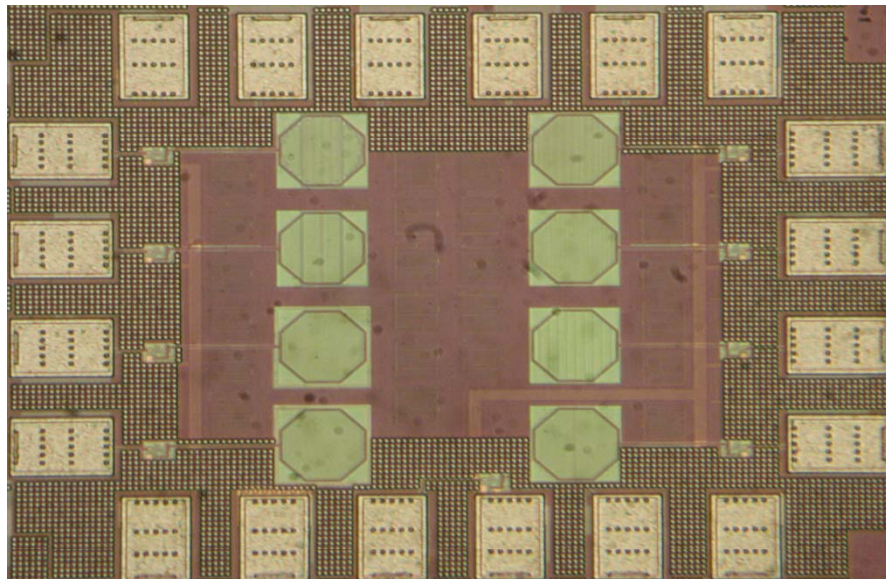
# Design

- A TIA is also integrated with each photodiode
- Reference TIA is also integrated for accurate de-embedding



# Design

- Manufactured in STM 65nm CMOS process
- No process modifications
- Silicide blocking layer is used
- 0.4mm<sup>2</sup> including pads

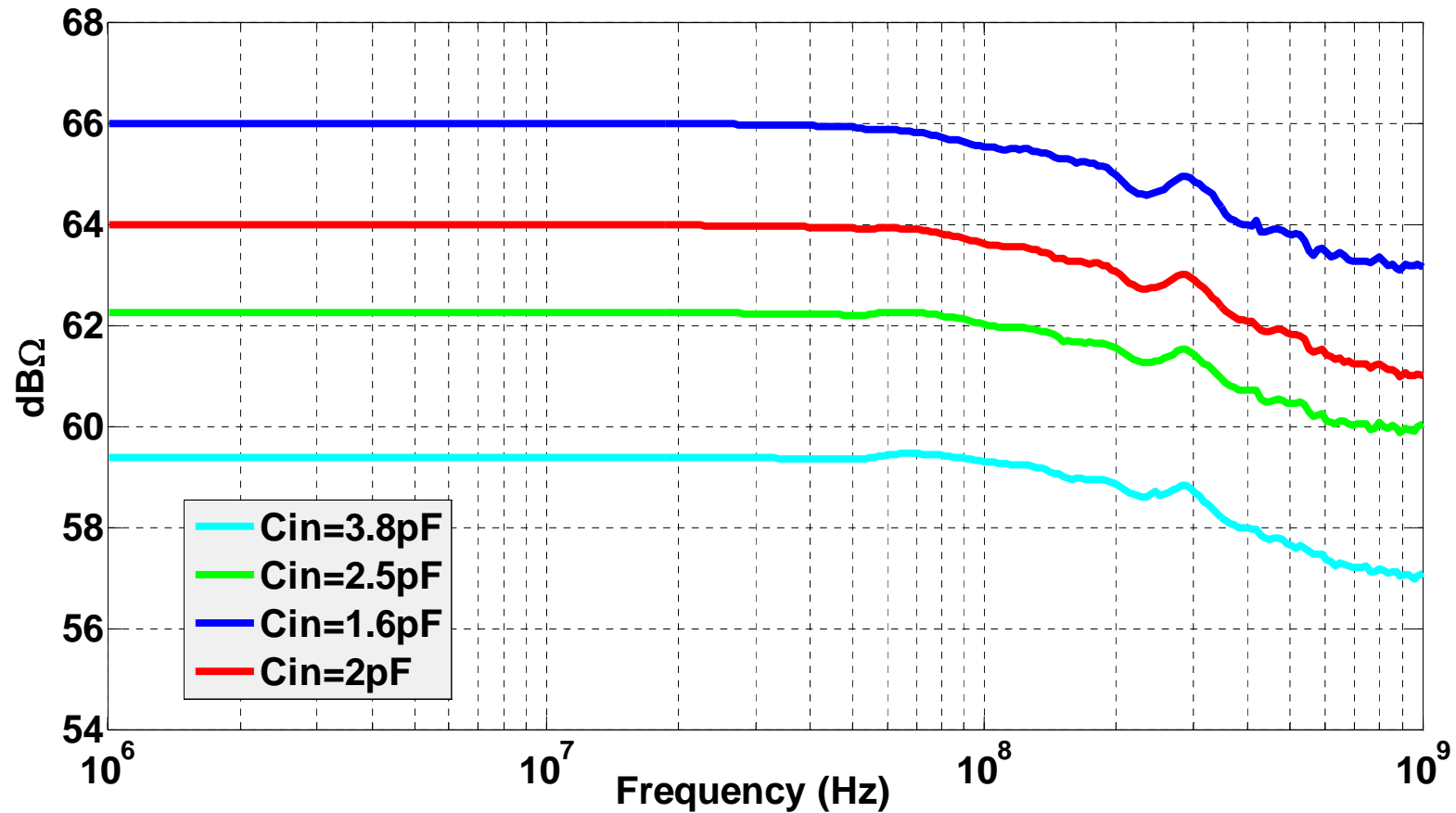


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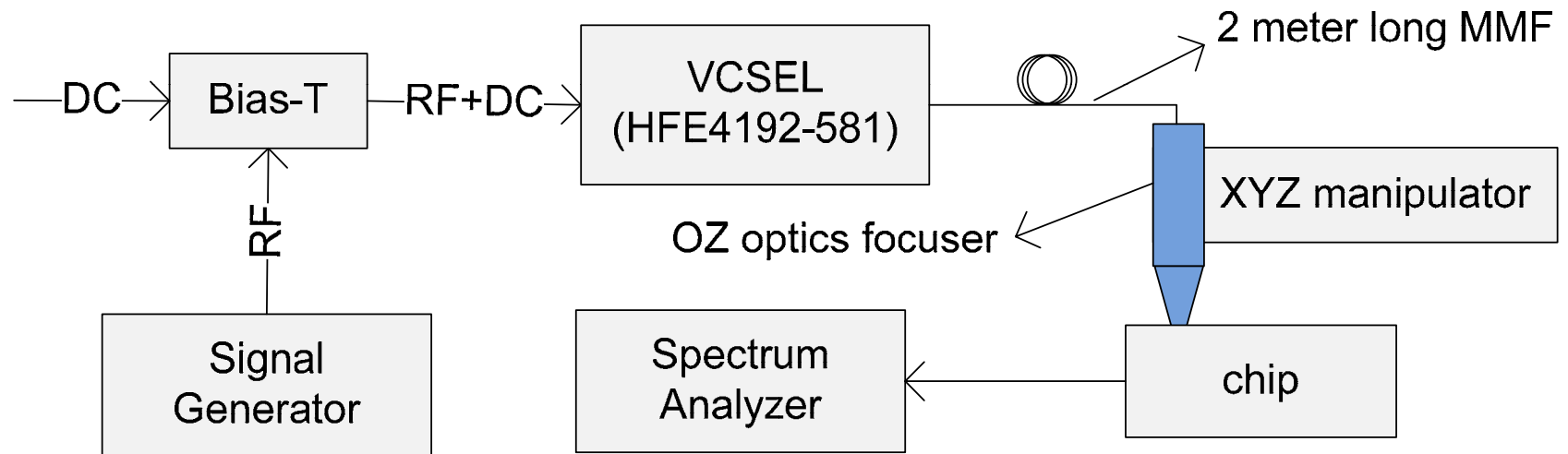
# Measurements

- Reference TIA is first measured



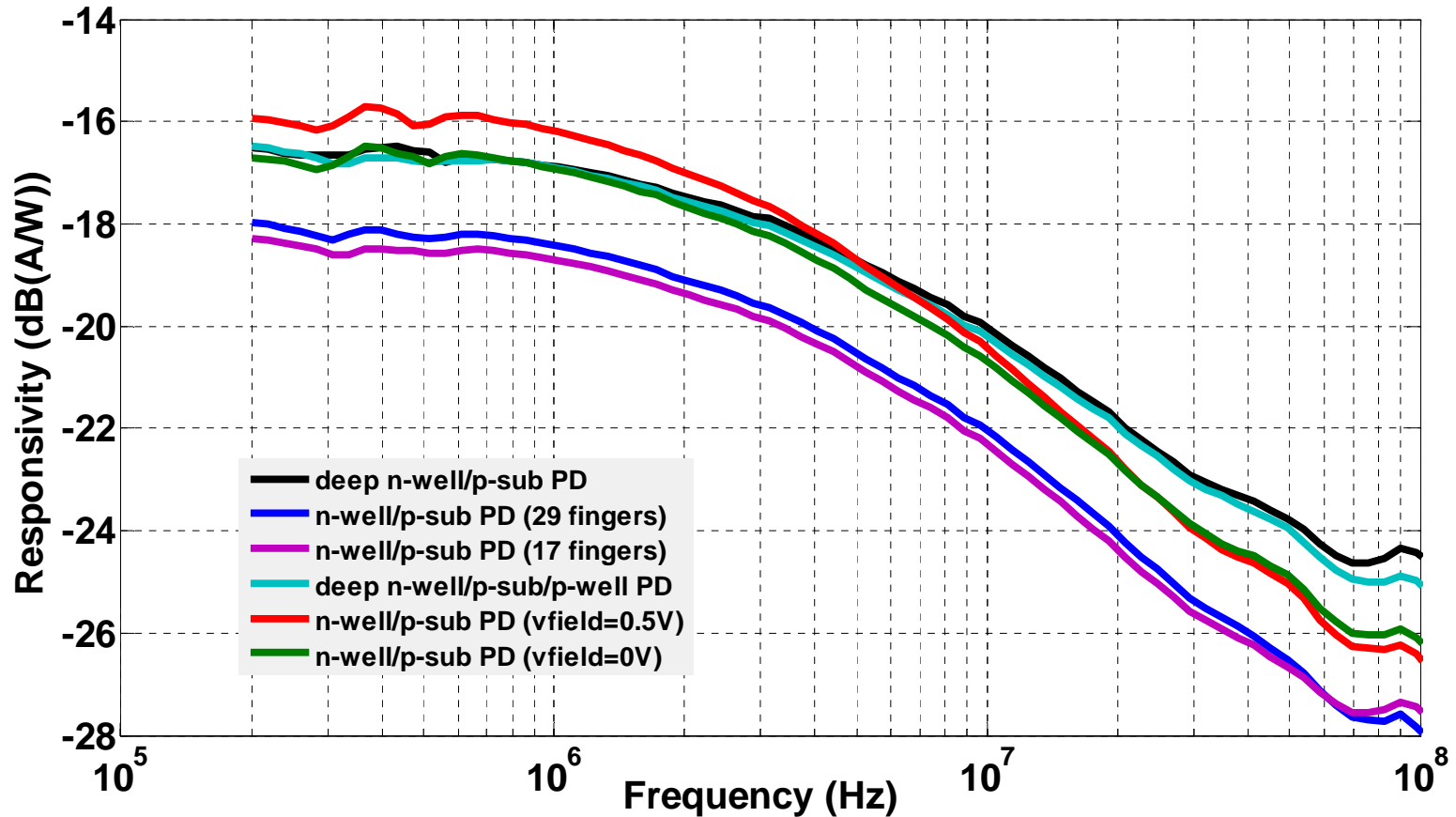
# Measurements

- Optical Measurement setup



# Measurements

- Measured frequency response





# Measurements

- Performance summary

Photodiode	Responsivity [A/W]	Bandwidth [MHz]	Roll-off [dB/decade]
n-well/p-sub	0.121-0.126	6.25	6
DNW/p-sub/p-well	0.15	6.8	5
DNW/p-sub	0.15	6.25	5
N-well/p-sub with electric field(0V/0.5V)	0.146/0.16	6.25/5.7	5.5/6

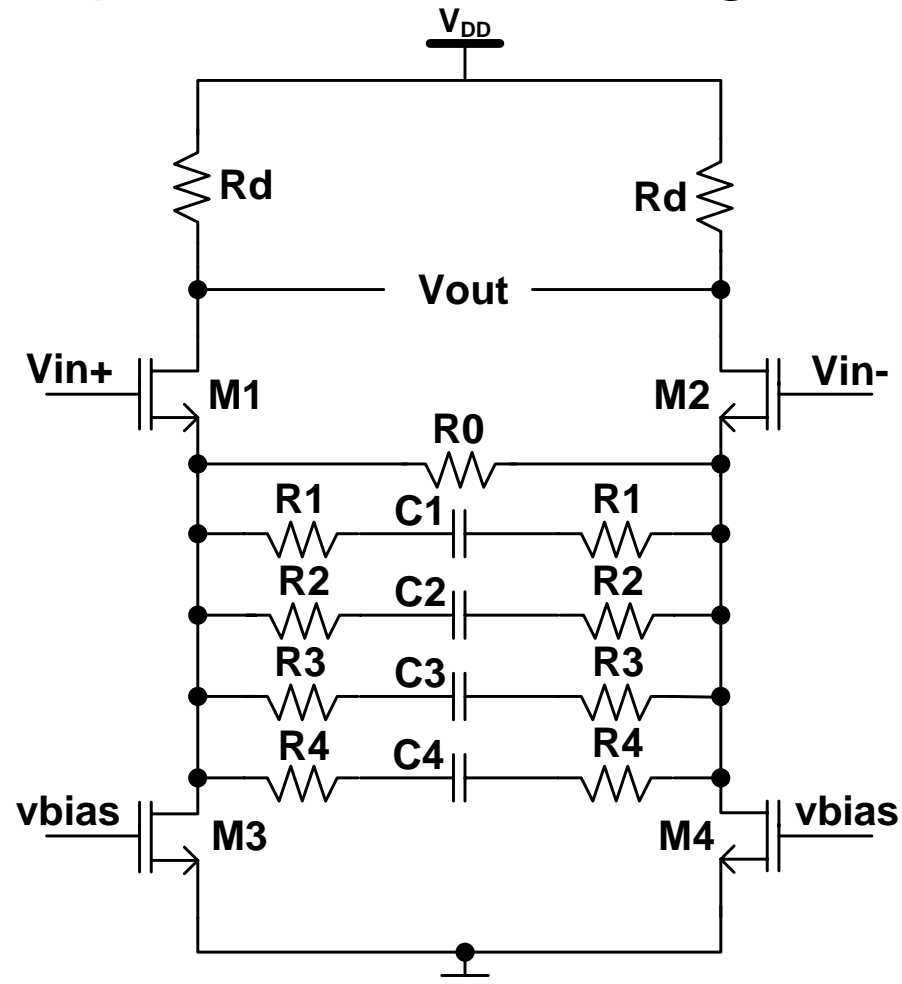
- Low roll-off=> equalization
- Analog equalizer for n-well/p-sub PD

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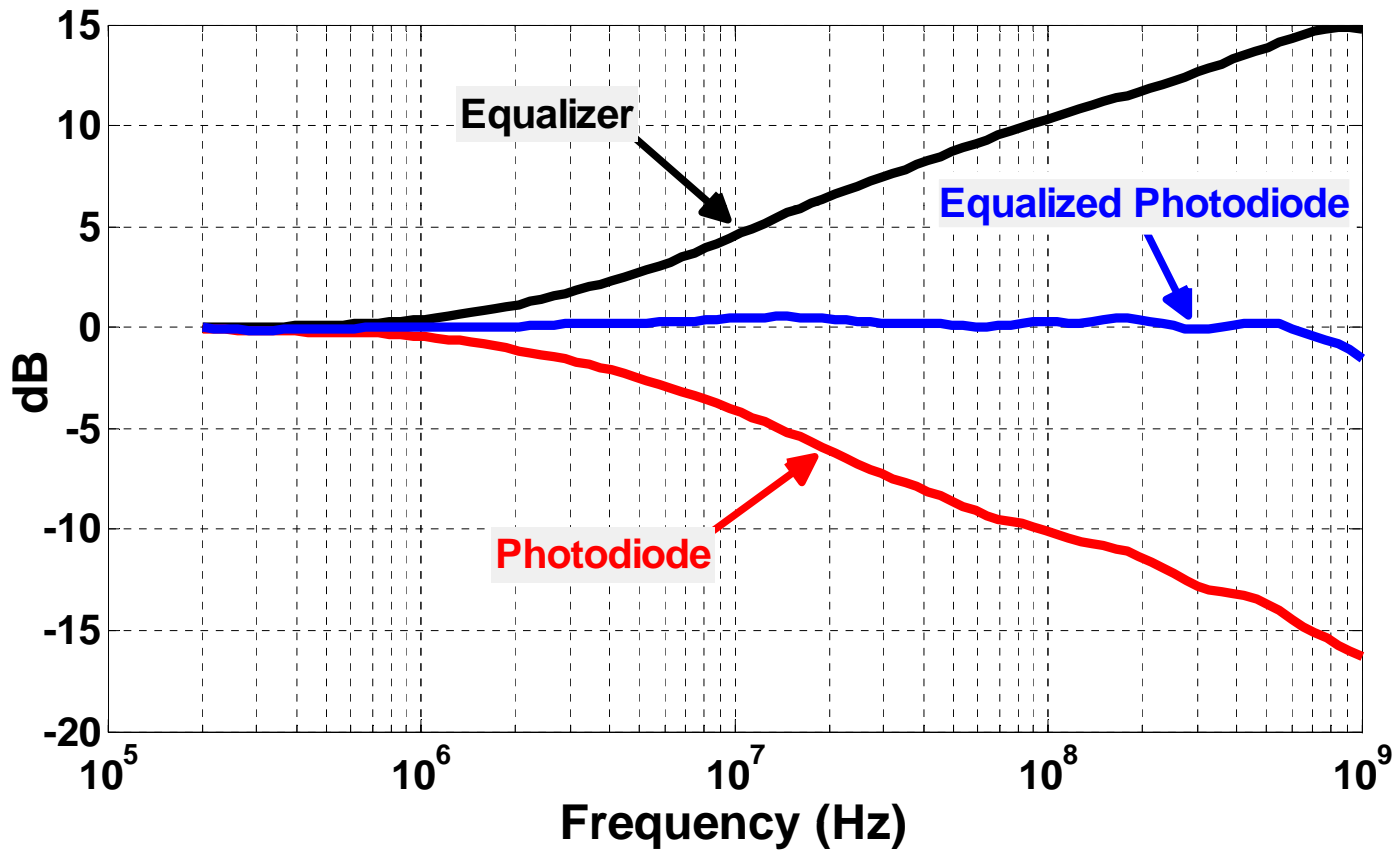
# Equalization of CMOS photodiodes

- Frequency dependent source degeneration



# Equalization of CMOS photodiodes

- Simulation results



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# Conclusion

- Several n-well/p-sub PDs are characterized
- DC responsivity=0.121-0.16A/W
- BW= ~6 MHz with a roll-off =~5.5dB/decade
- Results are useful in TIA and equalizer design
- Analog equalizer is designed

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