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Low Frequency Noise in Strained Silicon Nanowire Array MOSFETs and Tunnel-FETs

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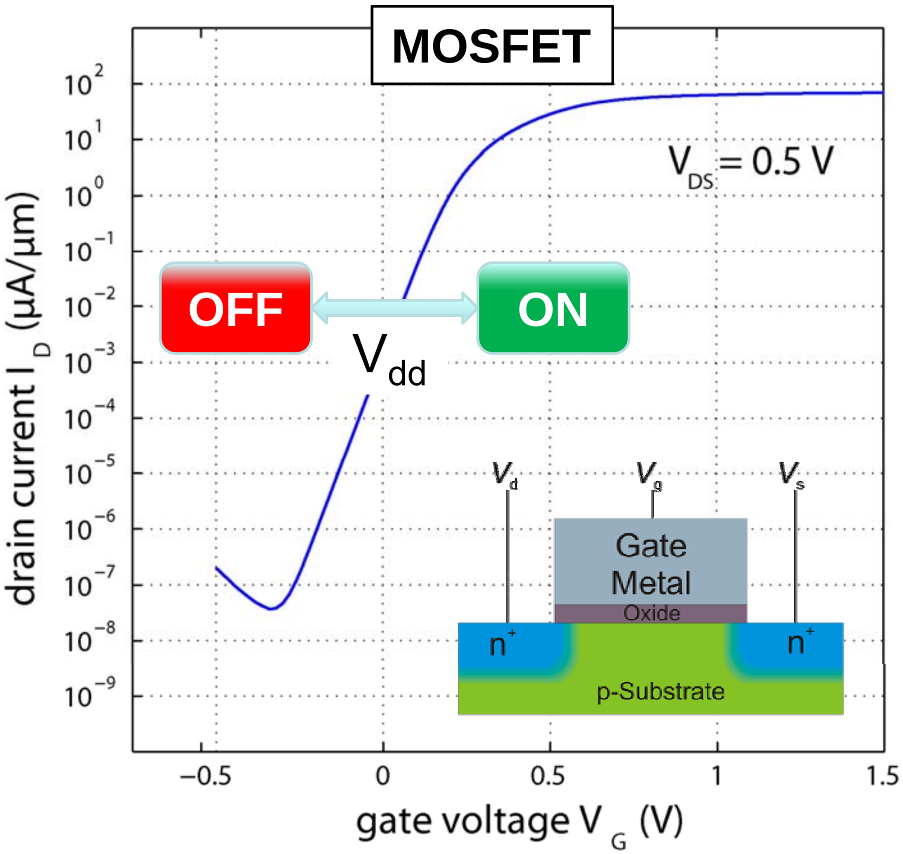
Outline

- Introduction
  - *Comparison of TFET and MOSFET*
- Device Fabrication
- DC Characterization
  - *MOSFET*
  - *TFET*
- Low Frequency Noise
  - *Measurement Setup*
  - *MOSFET*
  - *TFET*
- Conclusion

Research Motivation for Tunnel FET

MOSFET limitation: $S_{\mathrm{MOSFET}} = \frac{k_B T}{q} \cdot \ln(10) \approx$ 60 mV/dec at 300K



Dynamic power dissipation (charging, uncharging):

$$P_{dynamic} = C_{load} \cdot V_{dd}^2 \cdot f$$

Static Power:

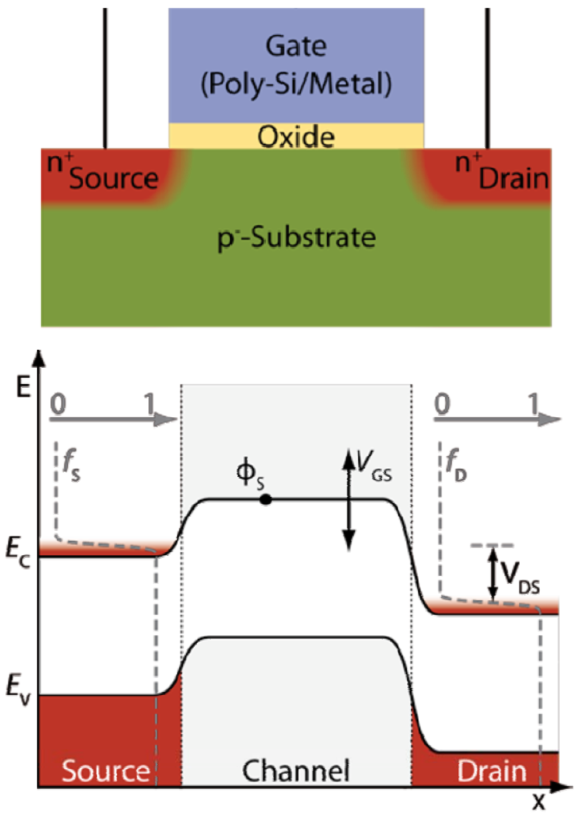
$$P_{static} = I_{off} \cdot V_{dd}$$

Steep switching slopes and low I_{off} reduce power consumption.

Tunnel field-effect transistor (TFET)

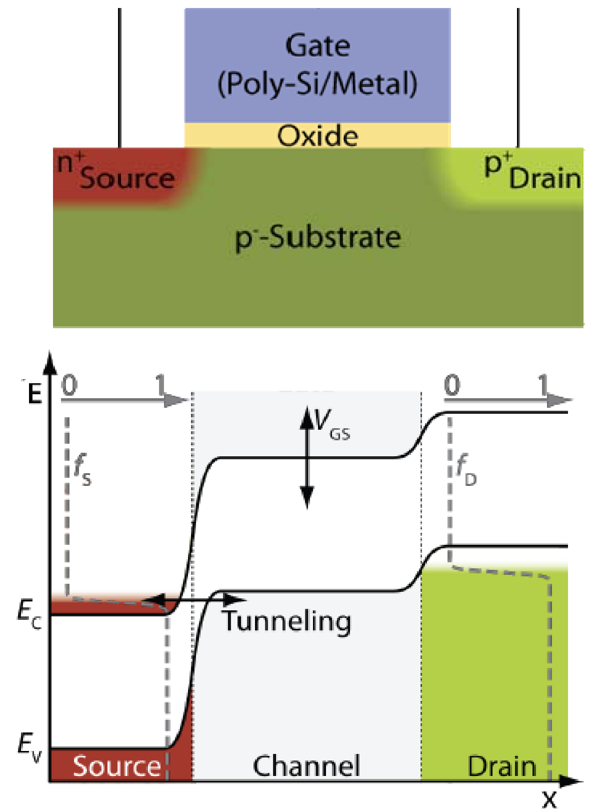
Carrier Transport

MOSFET



Thermal emission over potential barrier

Tunnel FET



Band-to-band tunneling

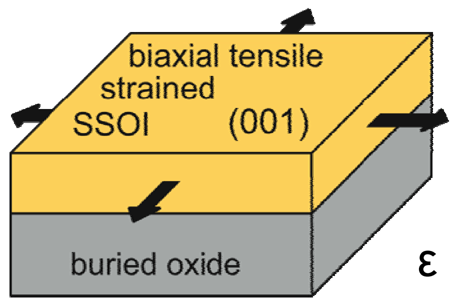
Study low frequency noise in MOSFET and TFET devices

TFET Fabrication

$$I_{ds} \sim T_{\mathrm{WKB}} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{3/2}}{3q\hbar(\Delta\Phi + E_g)}\right)$$

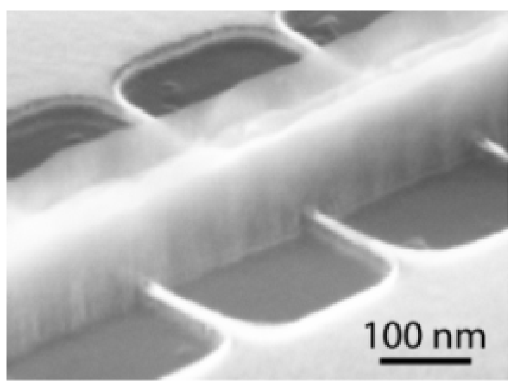
λ : Screening length of electrical potential
E_g: Bandgap
m*: Effective mass

- Decrease $\boldsymbol{E_g}$ and $\boldsymbol{m^*}$ by...
  - tensile strained SOI substrate

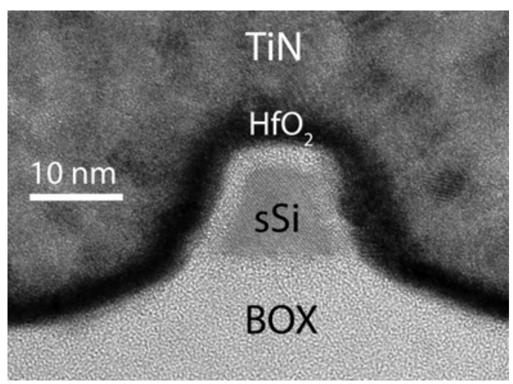


ε = 0.8 %

- Decrease **λ** by...
  - nanowire array
  - tri-gate
  - high-k dielectric

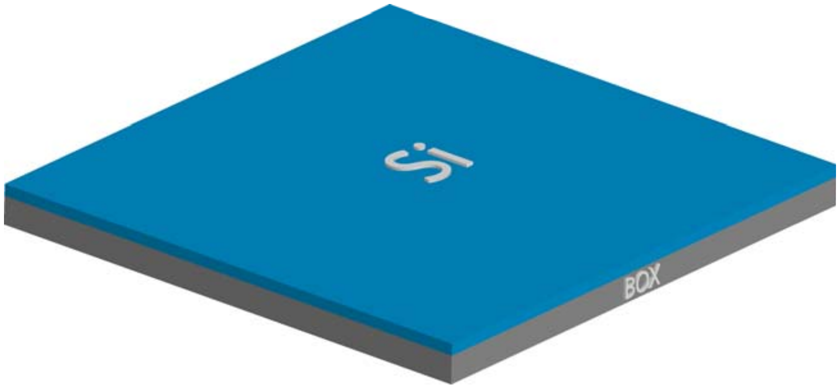


SEM: NW Array

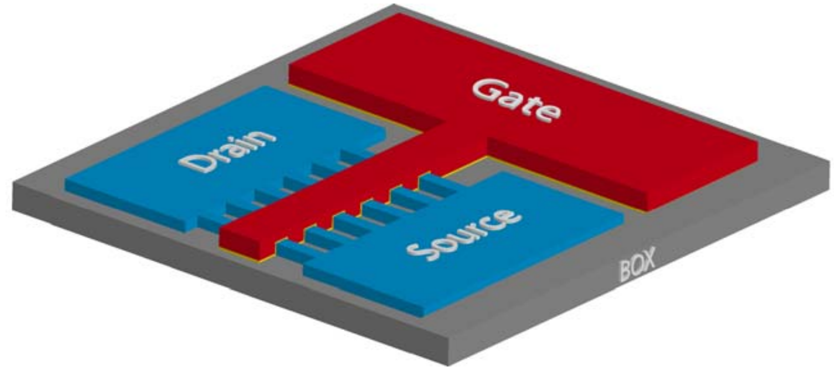


TEM: uniaxial strained NW

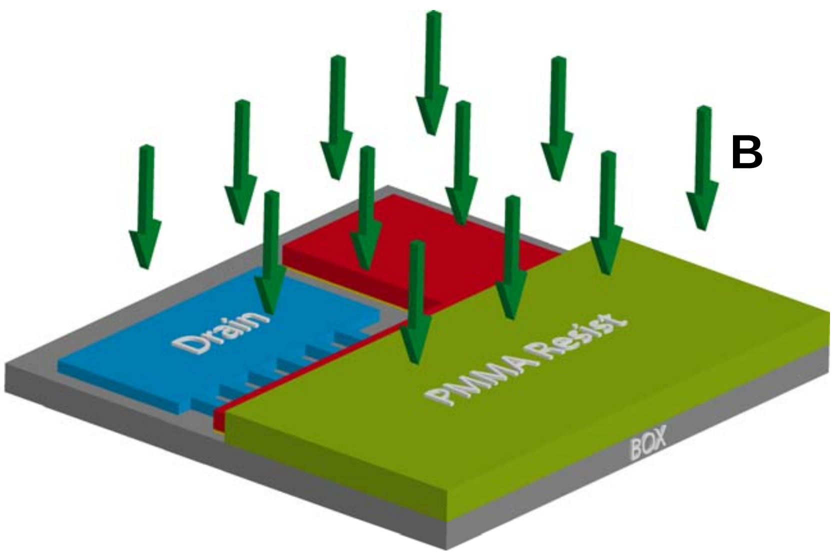
Process Flow Nanowire Array p-TFET



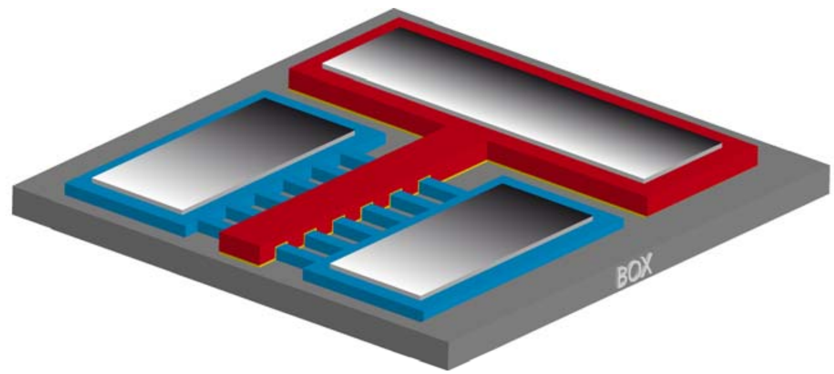
1. Patterning of the nanowire array



2. Deposition and patterning of the gate



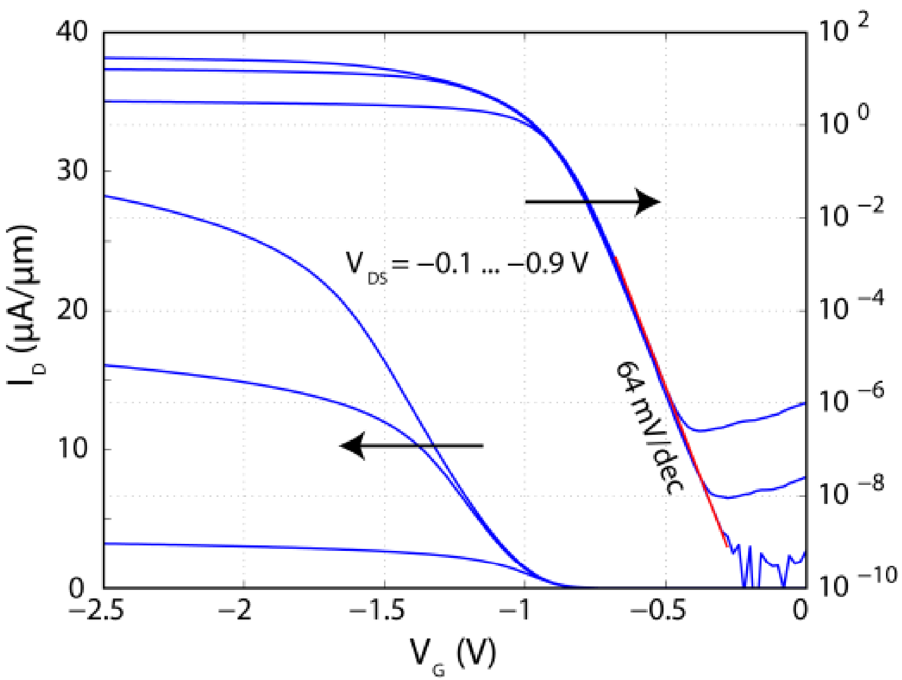
3. Source/drain implantation



4. Al contact formation

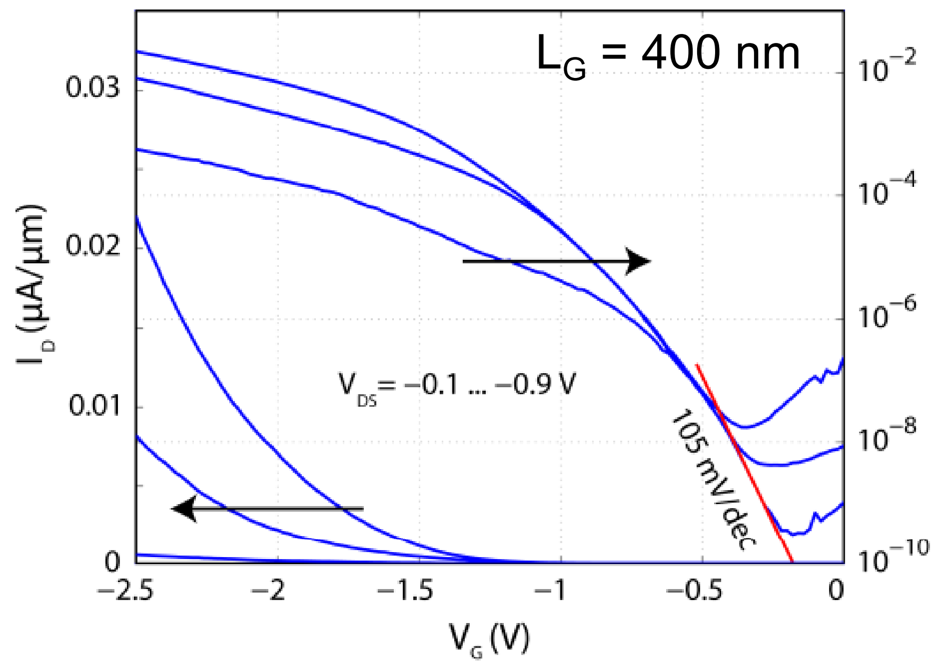
DC Transfer Characteristics

MOSFET



- *Close to ideal subthreshold slope*
- *$S \sim k_BT/q$, constant with V_G*
- ➢ *Good electrostatic gate control*

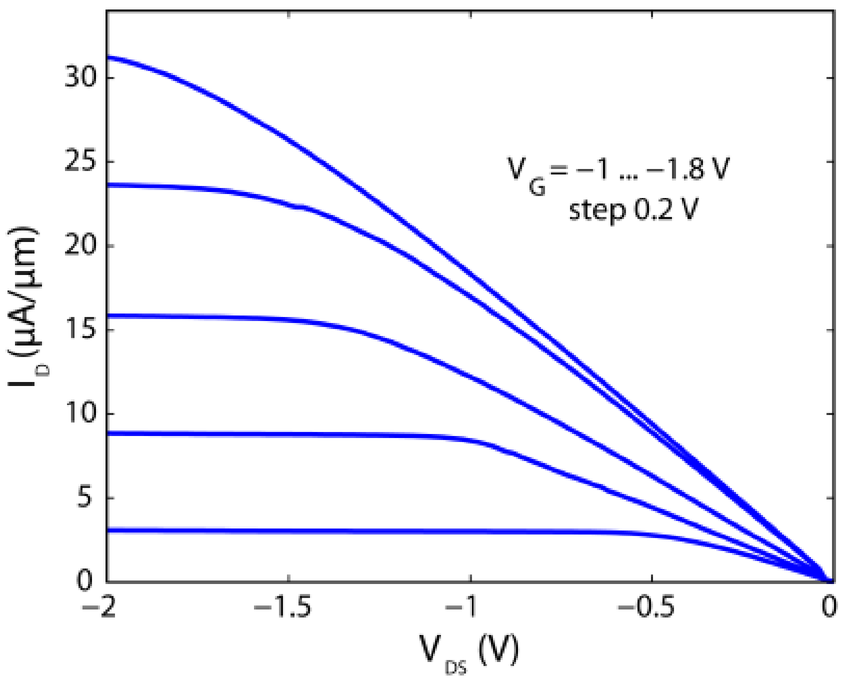
TFET



- *$S \sim \Delta\Phi \sim V_G$*
- *S > 60 mV/dec*
- ➢ $\lambda = \lambda_{channel} + \lambda_{junction}$

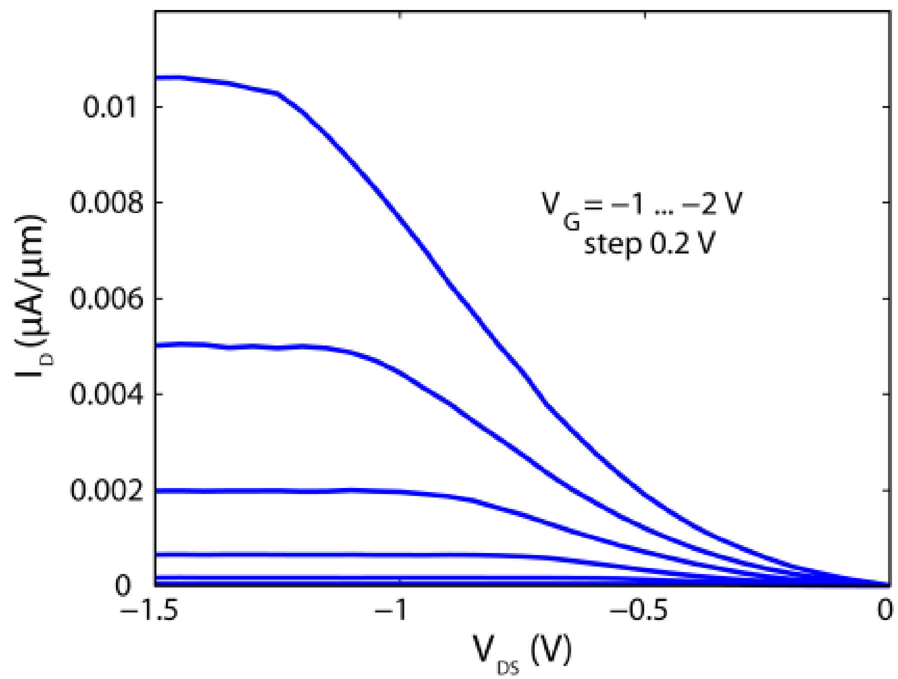
DC Output Characteristics

MOSFET



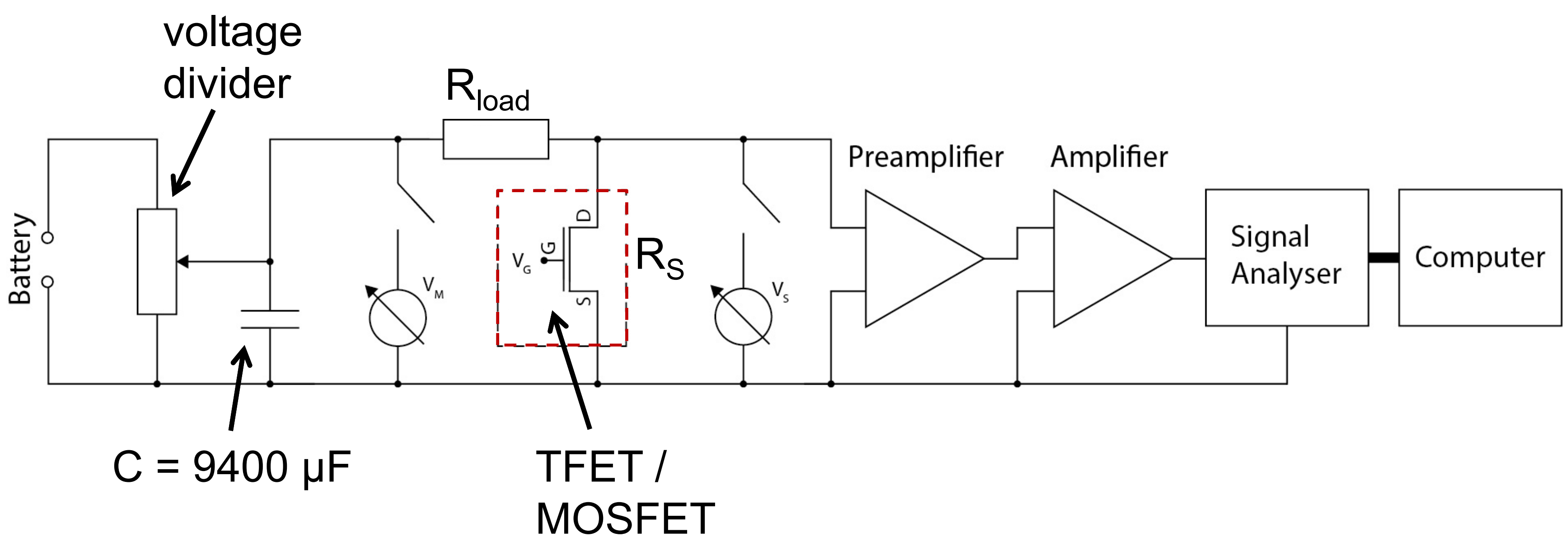
- *Channel and access resistance are major resistances*
- *Linear onset*
- *Linear increase with V_G*

TFET



- *Tunnel junction is major resistance*
- *S-shaped onset*
- *Exponential increase with V_G*

Setup – Low Frequency Noise

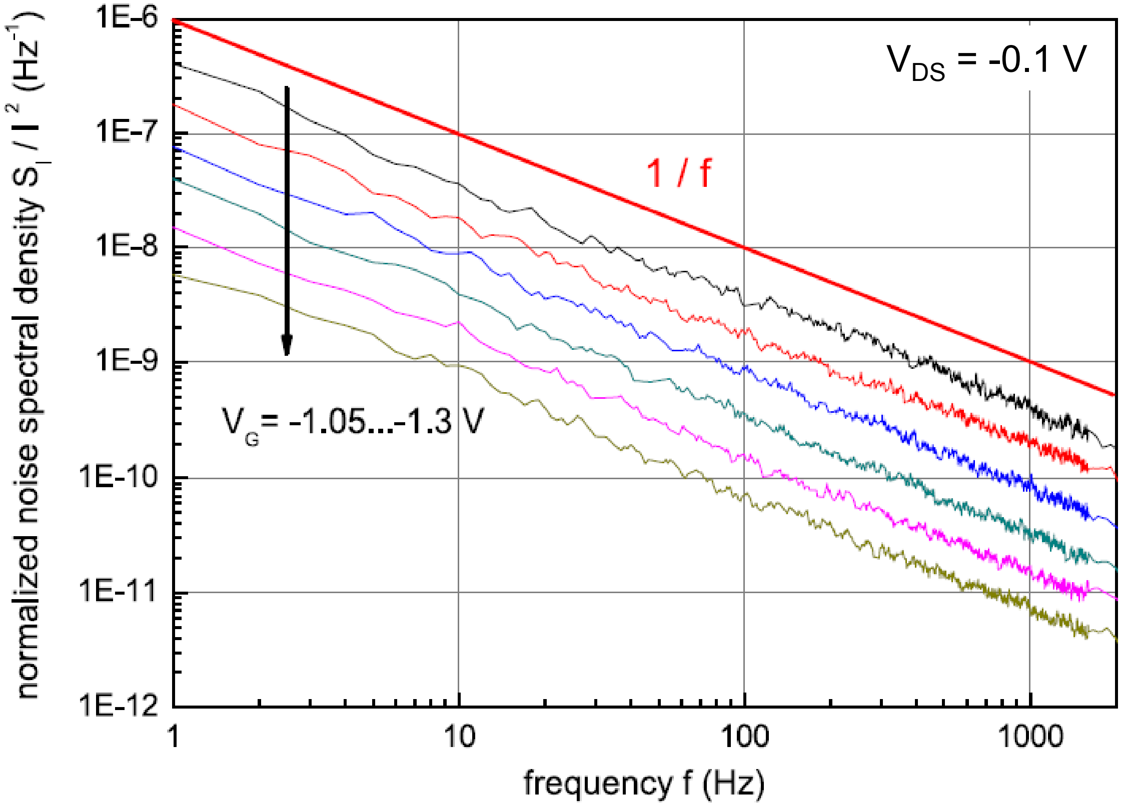


- Battery as source for V_G and V_{DS}
- R_{load} and R_S connected in parallel (AC signal)

$$\frac{R_{load}}{R_s} < \frac{1}{10}$$

- Voltage noise power spectral density measured
- Noise contribution of amplifiers calibrated and subtracted

Low Frequency Noise – MOSFET



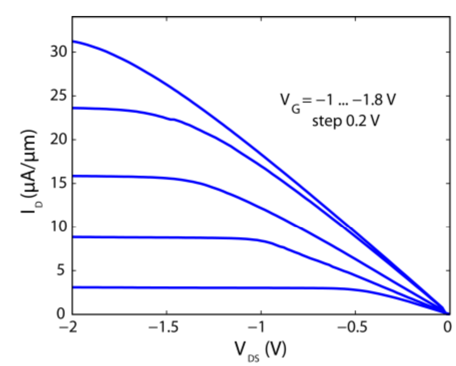
Current noise spectral density:

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2}$$

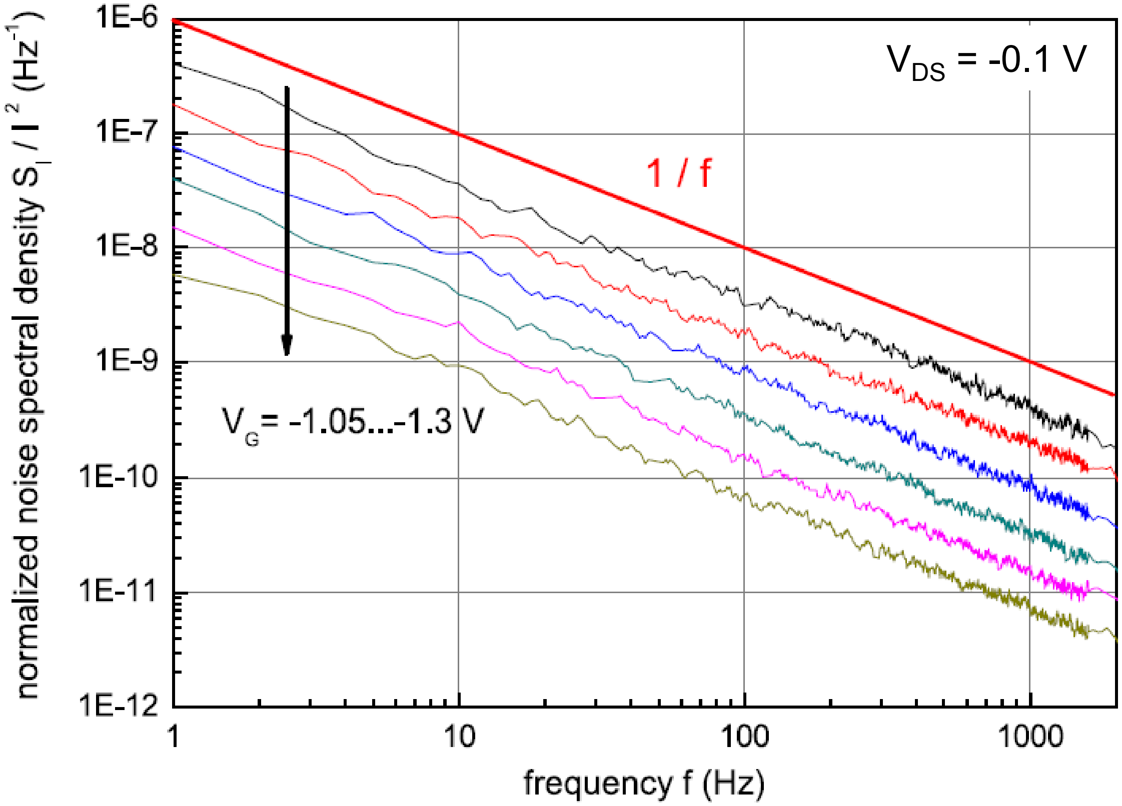
$$S_I(f) = S_V(f) \cdot \frac{I^2}{V^2} = \frac{S_V(f)}{R_{total}^2}$$

$$R_{total} = \left(\frac{1}{R_s} + \frac{1}{R_{load}}\right)^{-1}$$

- S_I calculated from S_V in the linear regime
- 1/f noise due to mobility fluctuations in the channel
- Depends on number of carriers in channel



Low Frequency Noise – MOSFET



Hooge empirical relation [1]:

$$\frac{S_I(f)}{I^2} = \frac{1}{f}\frac{\alpha_H}{N}$$

Hooge parameter:

$$\alpha_H = \frac{S_I f L^2}{q\mu I_D V_D}$$

$$\alpha_H = 7.3 \times 10^{-3}$$

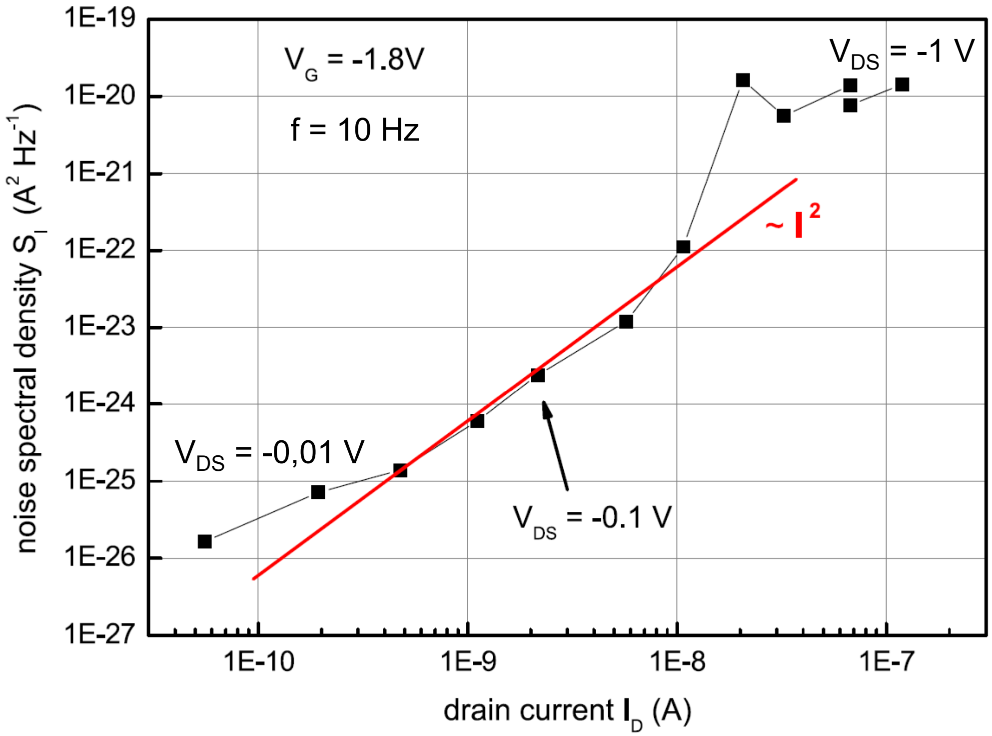
- Typical α_H for high-k devices 10^{-3} to 2×10^{-2} [2], [3]
- Good noise characteristics of the MOSFET reference devices

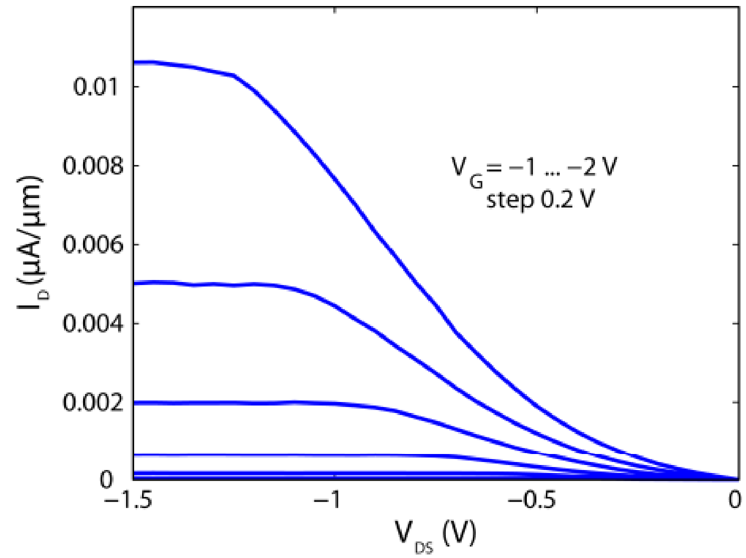
[1] Hooge et al., *Rep. Prog. Phys.* **44** p.479 (1981)
[2] Giusi et al., IEEE EDL **27** p.508 (2006)
[3] Simoen et al., APL **85 p.**1057 (2004)

Low Frequency Noise – TFET

Current noise spectral density:

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2} = \frac{c}{f} \quad \text{(in linear regime)}$$

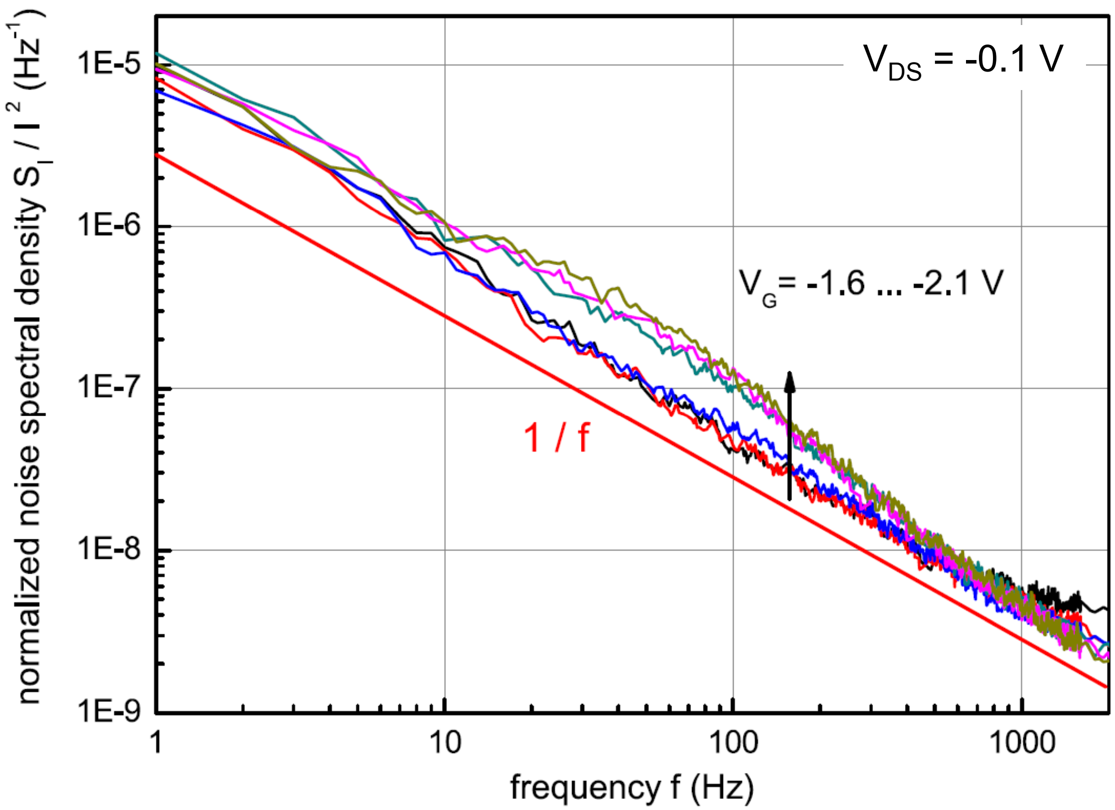




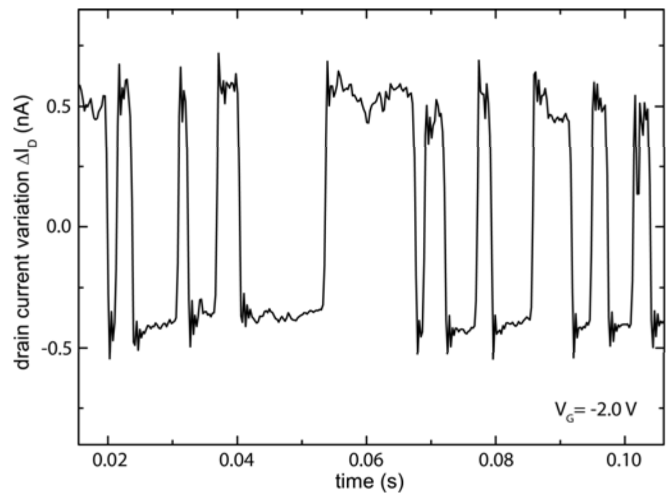
Where is the linear regime of the S-shaped output ?

- Check for linear dependence of S_I vs I_D^2
- V_{DS} = -0.1 V

Low Frequency Noise – TFET



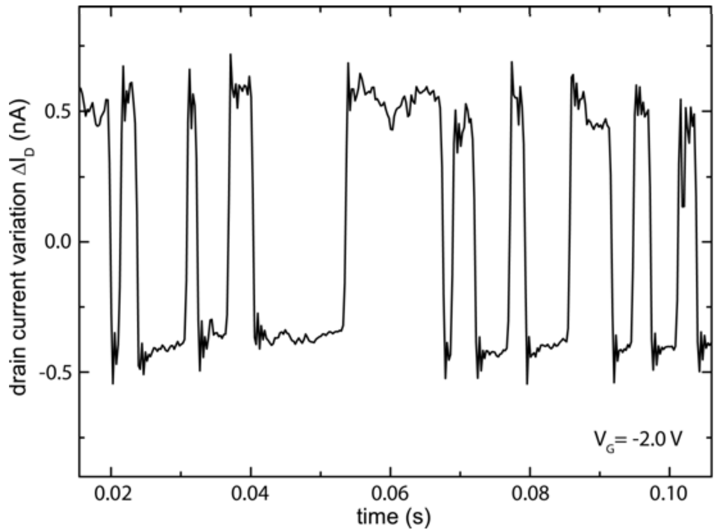
Time trace at V_G = -2 V



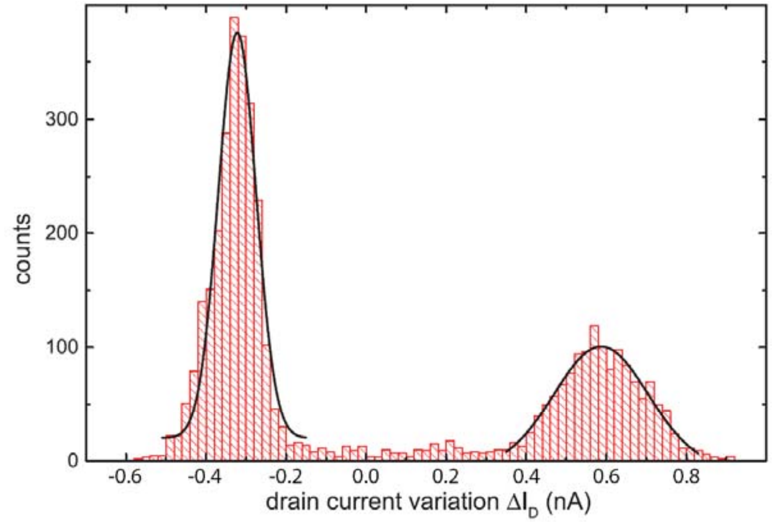
- S_I/I_D^2 constant with V_G for -1.6 V to -1.8 V
- Shape of spectrum changes abruptly
- Random Telegraph Signal (RTS) in time trace from $|V_G|$ > 1.9 V

RTS Noise – TFET

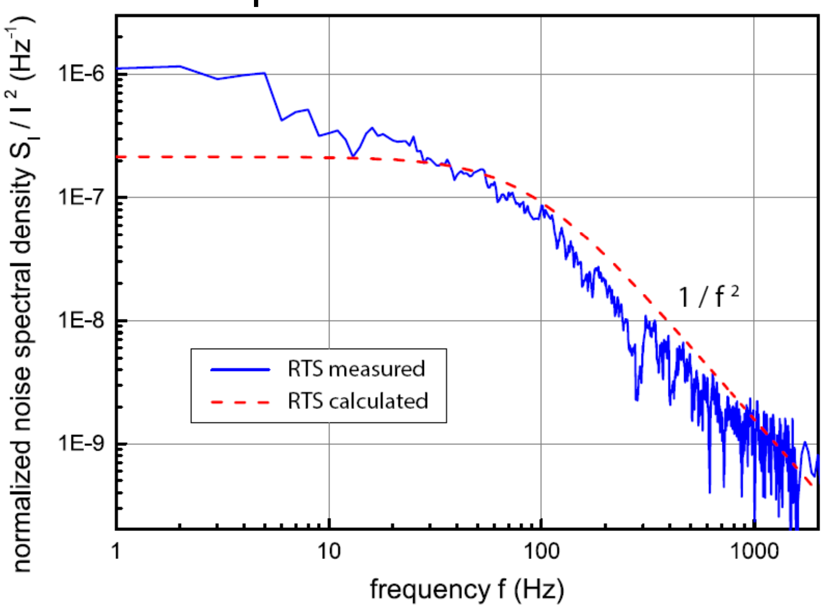
Time trace



Histogram of time trace



RTS spectrum



$$\tau_{down} = 5.12\,\mathrm{ms} \quad \tau_{up} = 2.88\,\mathrm{ms}$$

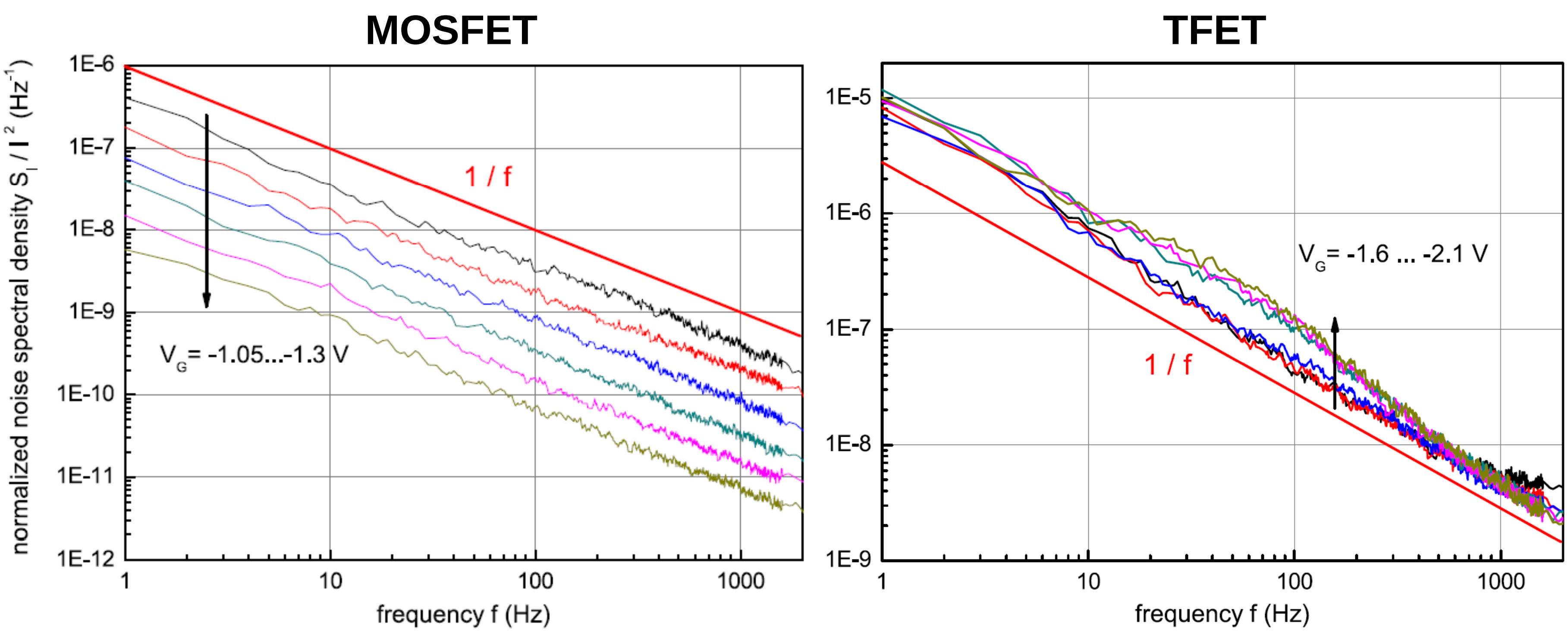
$$f_c = \tau_{up}^{-1} + \tau_{down}^{-1} = 542\,\mathrm{Hz}$$

Two level RTS noise [1]:

$$S_I(f) = 4\Delta I^2 \frac{(\tau_{up}\tau_{down})^2}{(\tau_{up}+\tau_{down})^3} \frac{1}{1+4\pi f^2/f_c^2}$$

[1] Yuzhelevski et al., Rev. Sci. Instrum. **71** 1681, 2000

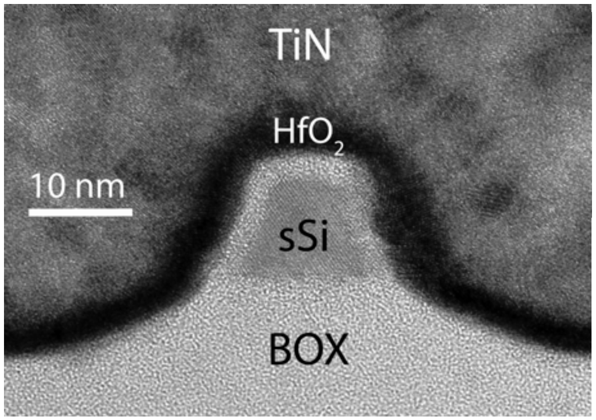
LFN – MOSFET vs TFET

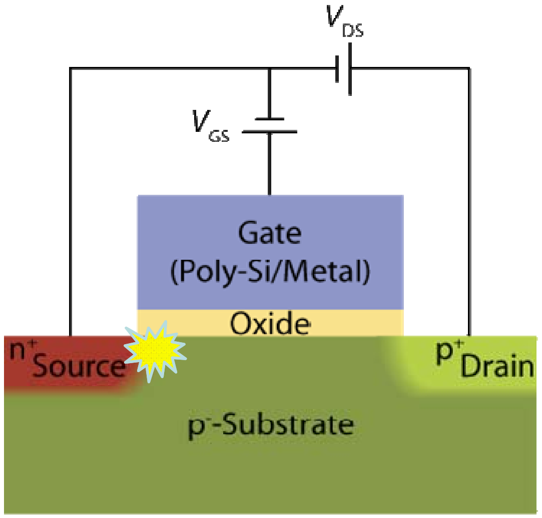


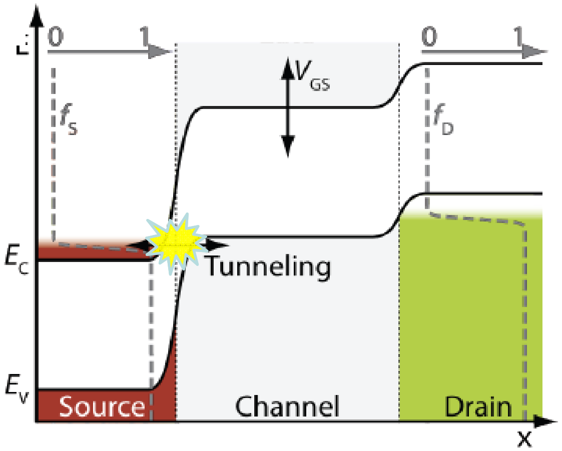
- Noise level in TFET higher than MOSFET
- No dependence on number of carriers in channel in TFET
  - ➢ Tunnel junction is the main source of noise in the TFET

Origin of RTS Noise in TFET

- RTS noise in MOSFETs observed for small gate area / short channels
- Confined tunnel junction area independent of gate length
- Exponential dependence of BTBT on gate potential

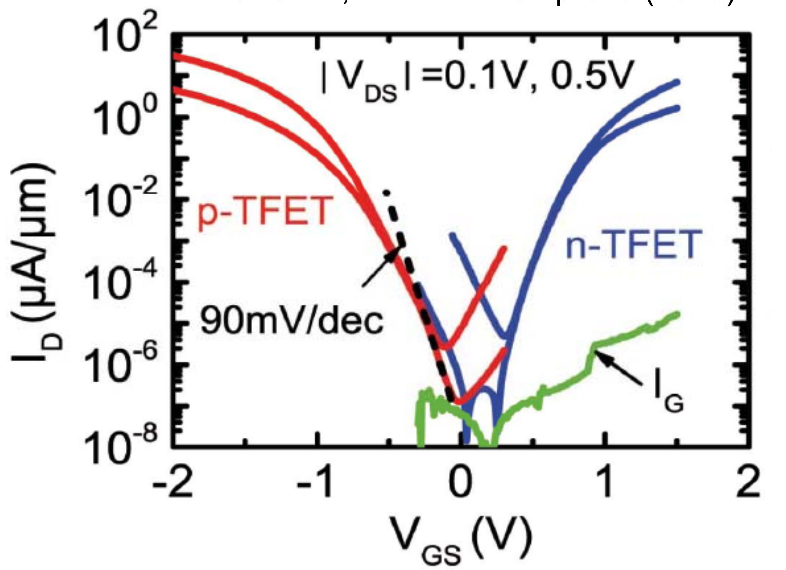


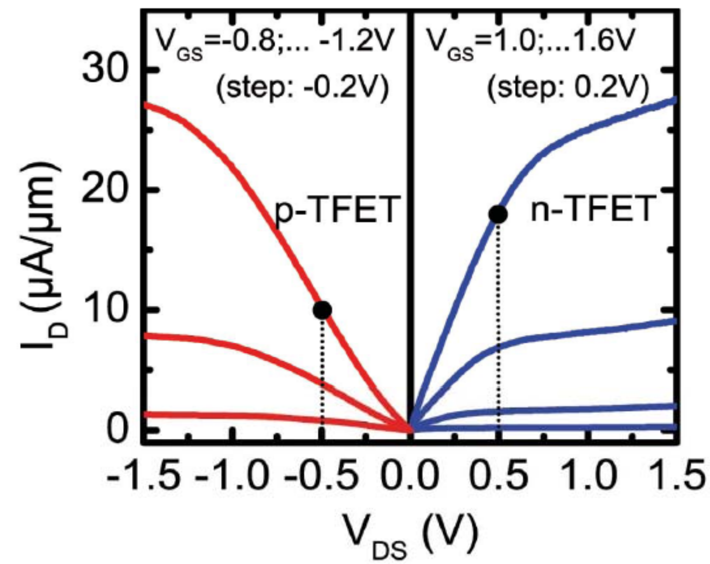


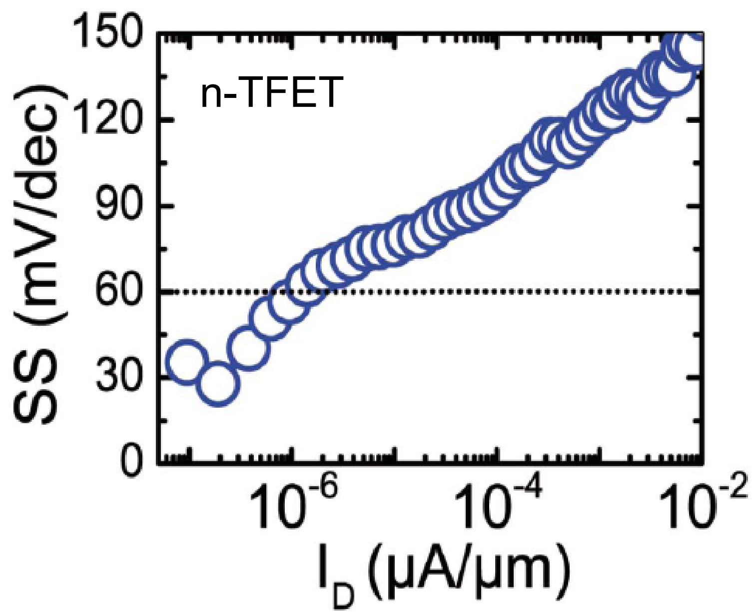


Outlook – Next Generation TFET

Knoll et al., IEEE EDL **34** p.813 (2013)







- Tunnel junction formation by dopant segregation
- Reduced trap assisted tunneling
- Improved on-current
- S < 60 mV/dec

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Conclusion

✓ *NW array MOSFET:*

- *Close to ideal inverse subthreshold slope*
- *Good noise performance*

✓ *NW array TFET:*

- *Exceeds MOSFET noise level*
- *Noise generated in tunnel junction*
- *Confined tunnel junction more likely to generate RTS noise*