ESSDERC Presentation

Effect of Ions Presence in the SiOCH Inter Metal Dielectric Structure

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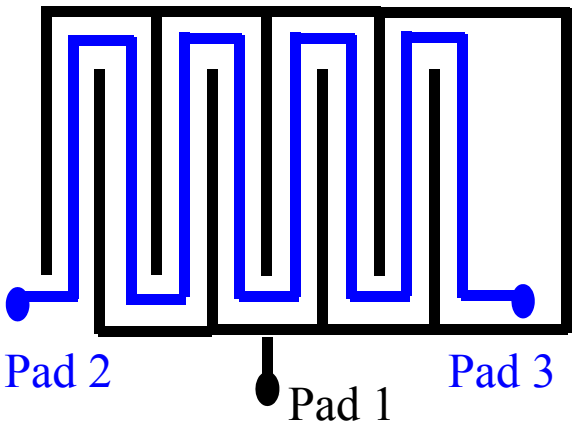
Summary

Context

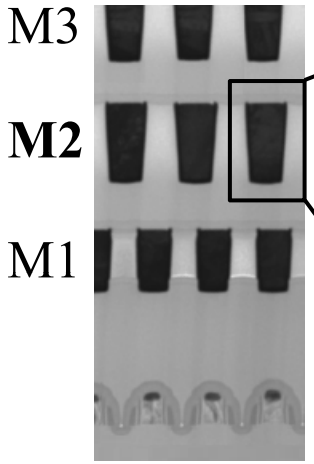
- Low-k dielectrics are used:
  - To reach the resistance capacitance (RC) reduction requirement for scaled down microelectronics devices
- Low-k dielectrics : reliability issue [1]-[4]
  - Lower dielectric strength
  - High leakage current
  - Premature breakdown
- Purpose :
  - Understand the conduction mechanisms into Inter Metal Dielectric (IMD) structure
  - Explain physically the high leakage current
  - Investigate time to breakdown issue

[1] E. T. Ogawa, IRPS, 2003
[2] K. Y. Yiang, Appl. Phys. Lett., 2003
[3] J. R. Lloyd, J. Appl. Phys., 2005
[4] G. G. Gischia, IRPS, 2010

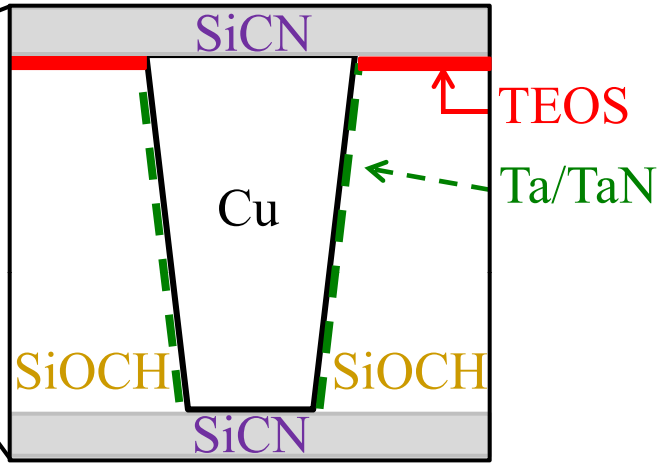
Technical details



Pad 1: Comb line
Pad 2&3 : Serpentine line



TEM cross section



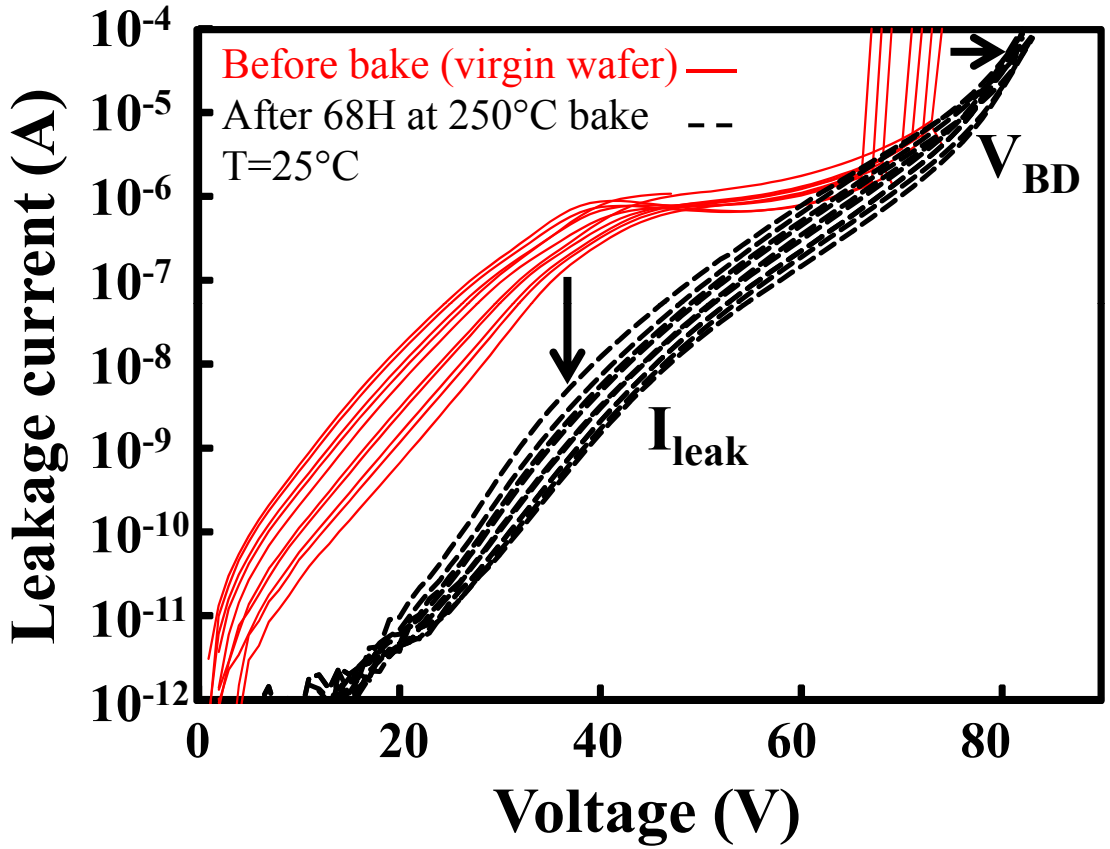
IMD structure stack

Experimental measurement

- Linear Ramp Voltage Stress (LRVS)
- Leakage current versus voltage applied (I-V)
- Time Dependent Dielectric Breakdown (TDDB)

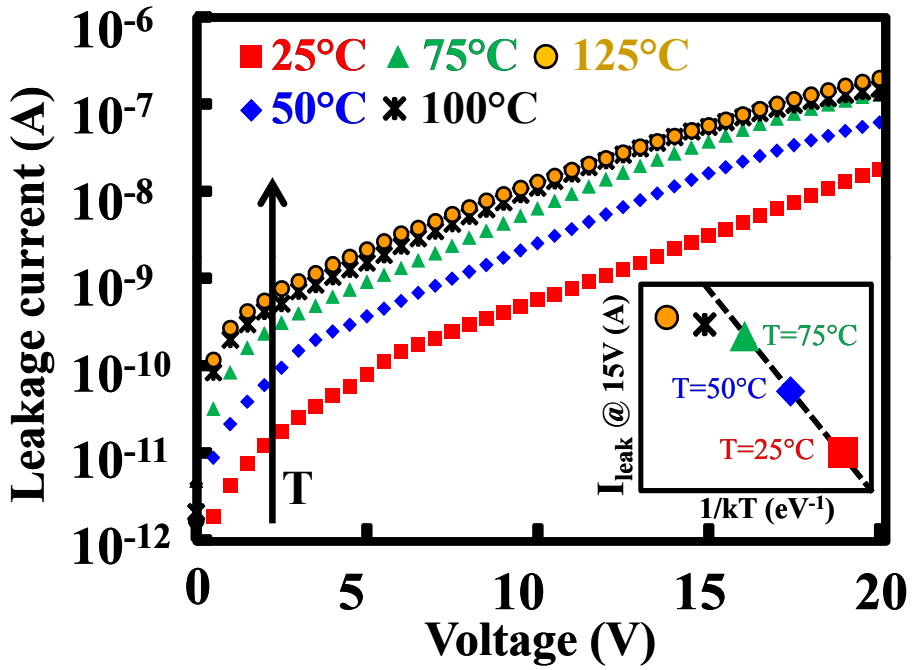
Summary

Bake impact



- Bake impact ➔ I_{leak} decreases and V_{BD} increases

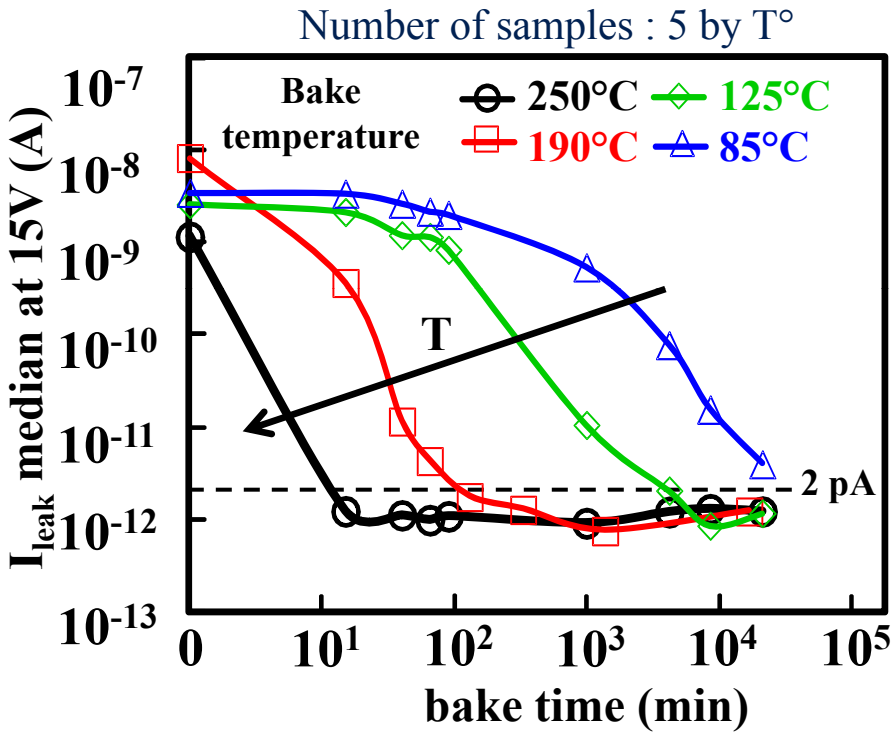
Temperature effect on I-V characteristics

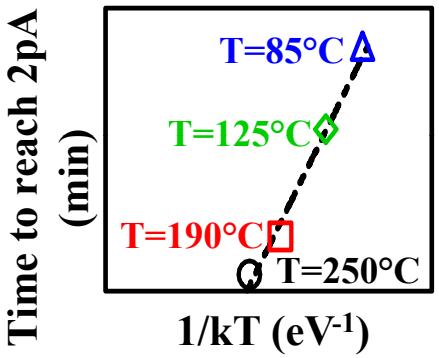


➔ E_a=0.45eV

- Temperature increasing ➔ Leakage current increasing
- E_a=0.45eV significant of a physical phenomenon
- High temperature (T>75°C)➔ Saturation phenomenon

Leakage annealing at high temperature

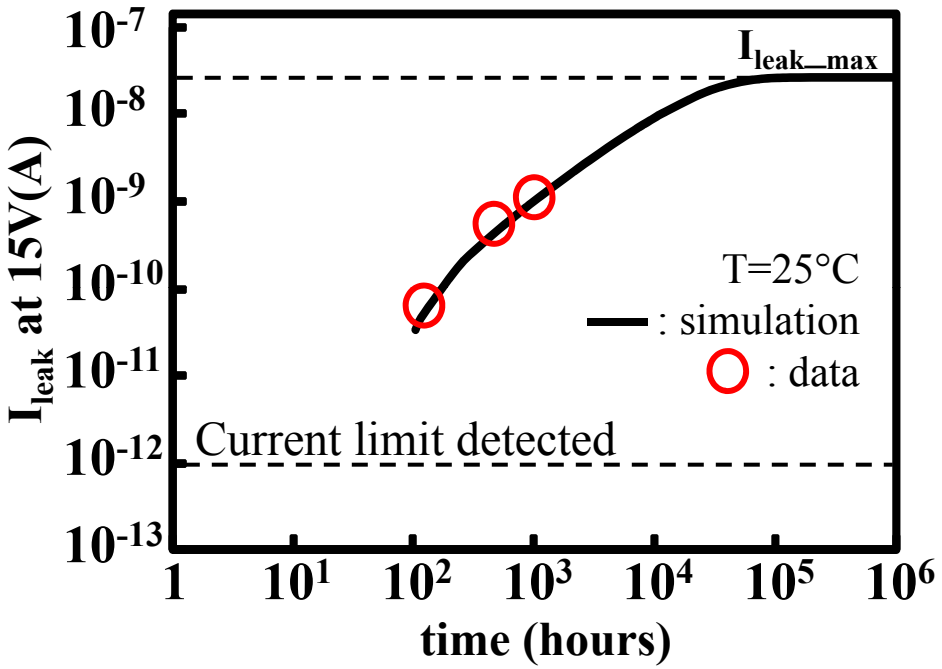




➔ E_a=0.75eV

- Bake temperature increasing ➔ Time to reach 2pA decreases
- Activation energy of leakage annealing = 0.75eV

Leakage kinetic at room temperature

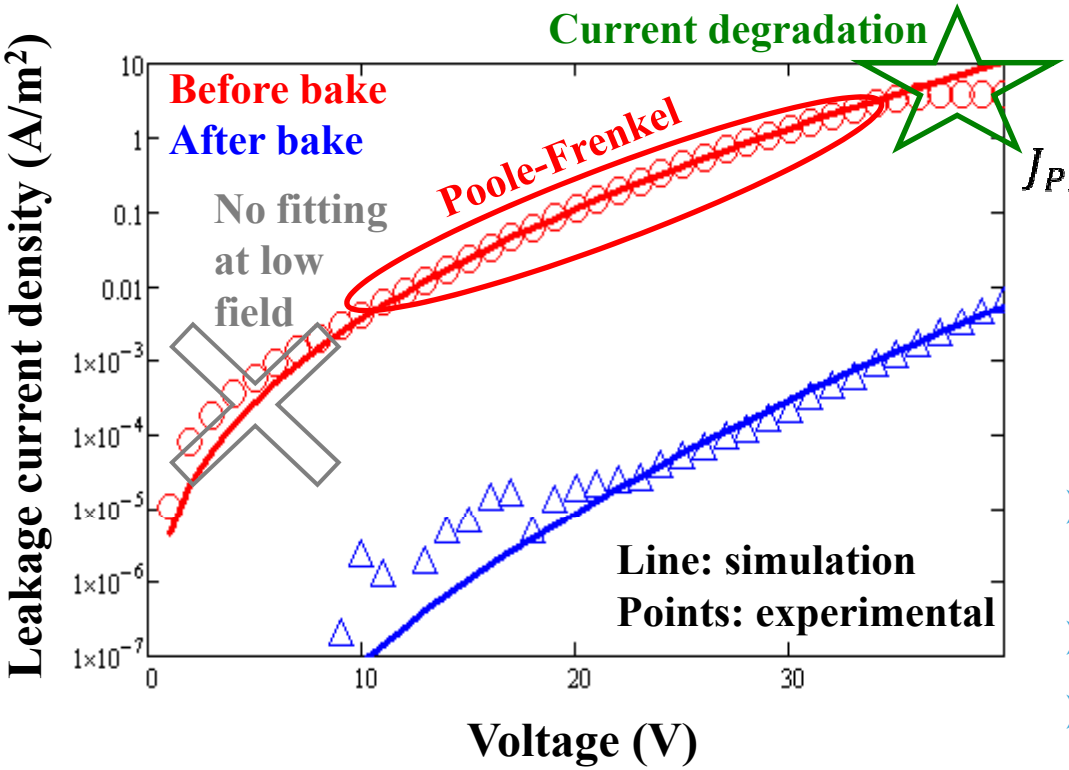


$$I_{leak} = I_{leak\_max} \times \left(1 - e^{-\left(\frac{t-t_0}{k}\right)}\right)$$

- Room temperature (25°C) ➔ leakage current increasing

Summary

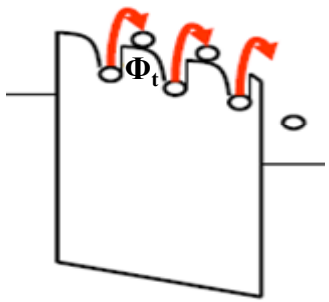
High field simulation



$$J_{PF} = A_{PF} \times \frac{V}{t_{OX}} \times e^{-\left(\frac{q \times \Phi t}{k \times T}\right)} \times e^{\left(\beta_{PF} \times \sqrt{\frac{V}{t_{OX}}}\right)}$$

$$\beta_{PF} = \sqrt{\frac{q^3}{\pi \times \varepsilon_0 \times K_{tox}}} \times \frac{1}{r_{SiOC} \times k \times T}$$

- A_{PF}: material conductivity : trap density and temperature dependent
- Φ_t: trap potential barrier height
- K_{tox}: relative dielectric constant



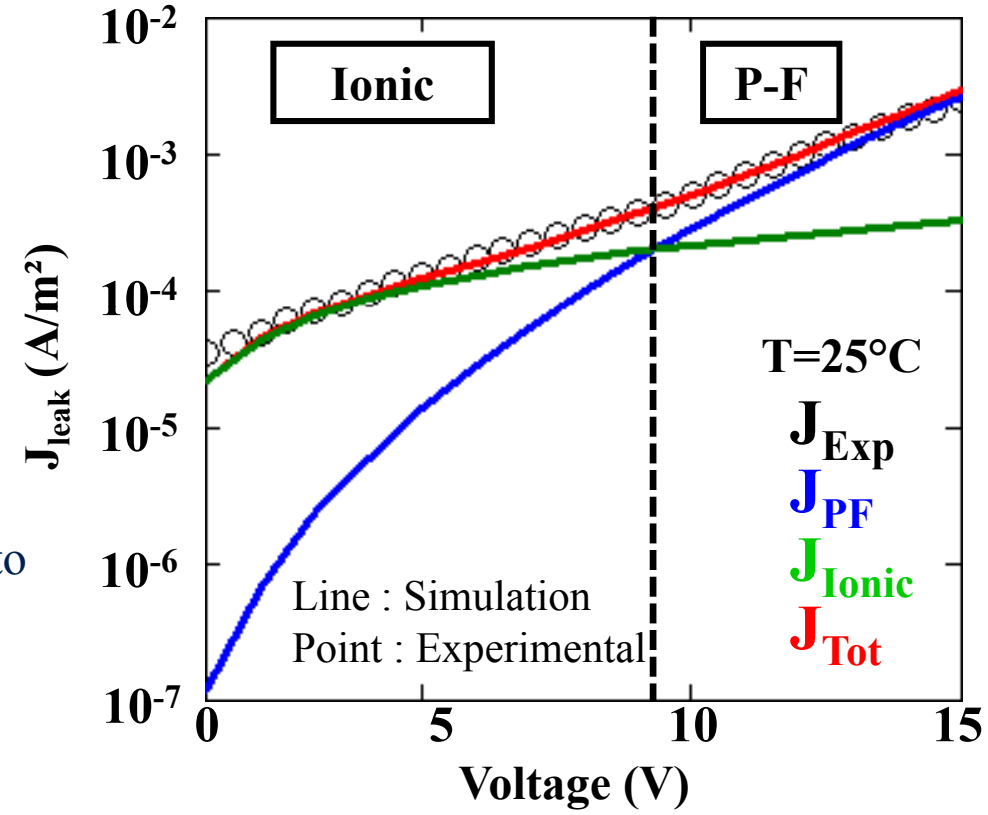
A_{PF} before bake	1.6×10^{-14} S/m
A_{PF} after bake	1.6×10^{-18} S/m

[5] M. Lin, EDL, 2003

Low field simulation

$$J_{ION} = \frac{A_{ION} \times V}{T \times t_{SiOC}} \times e^{-\frac{E_a}{k \times T}}$$

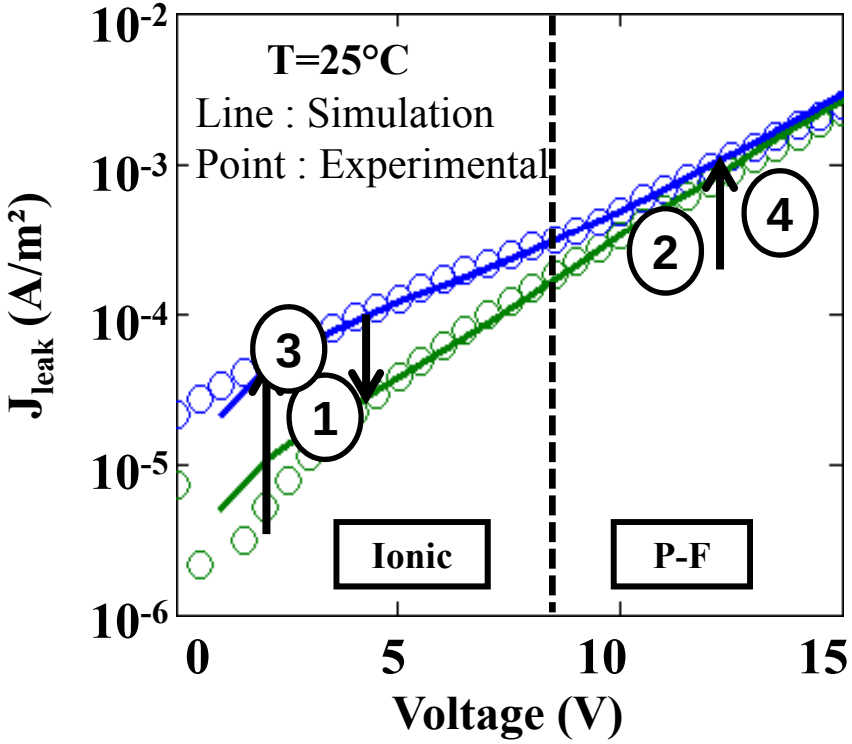
- A_{ION}: fitting parameter
- E_a: Ions activation energy extrapolated to **1.1eV** : alkaline ion (Na^+, K^+, H^+ etc…)

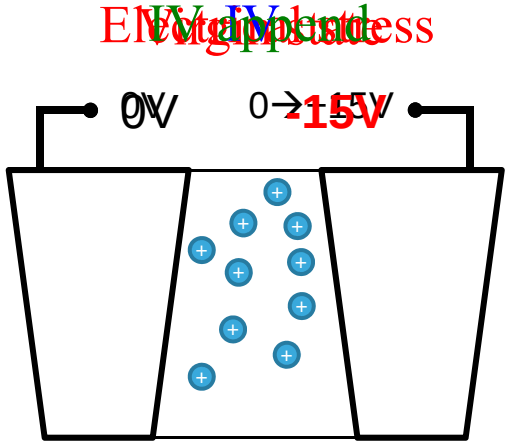


- Fitting at high field but not at low field

$$J_{Tot} = J_{Ionic} + J_{Poole\text{-}Frenkel}$$

Ions movement

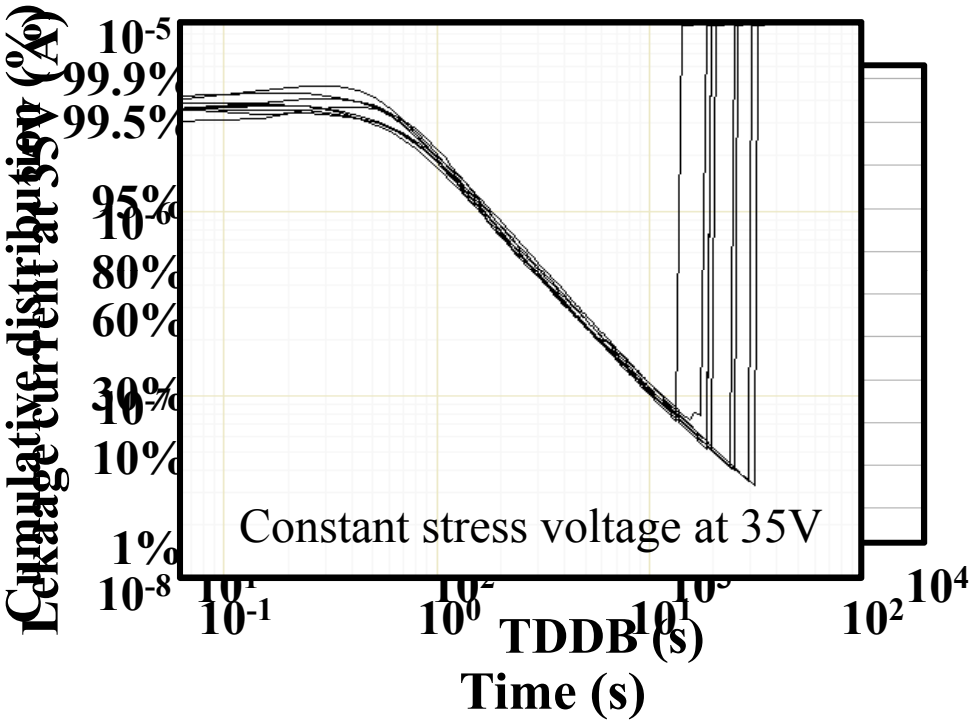


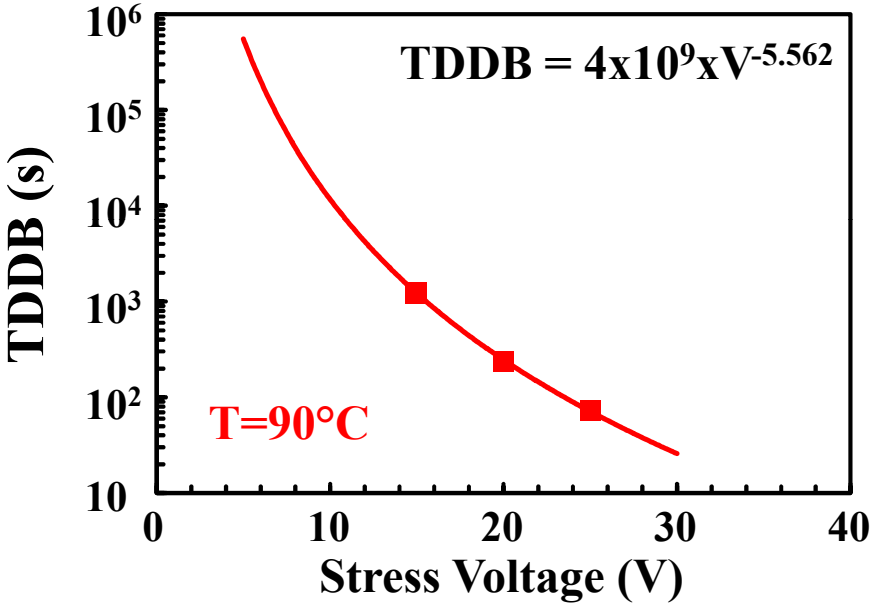


Parameters	Initial	After stress	Readout
A_{ION} (K·S/m)	$4.8x10^{3}$	$8.02x10^{4}$	$1.87x10^{4}$
A_{PF}(S/m)	$6.42x10^{-15}$	$2.67x10^{-14}$	$2.67x10^{-14}$

3. No more contribution of ions
4. Trap density increased due to applied electrical stress

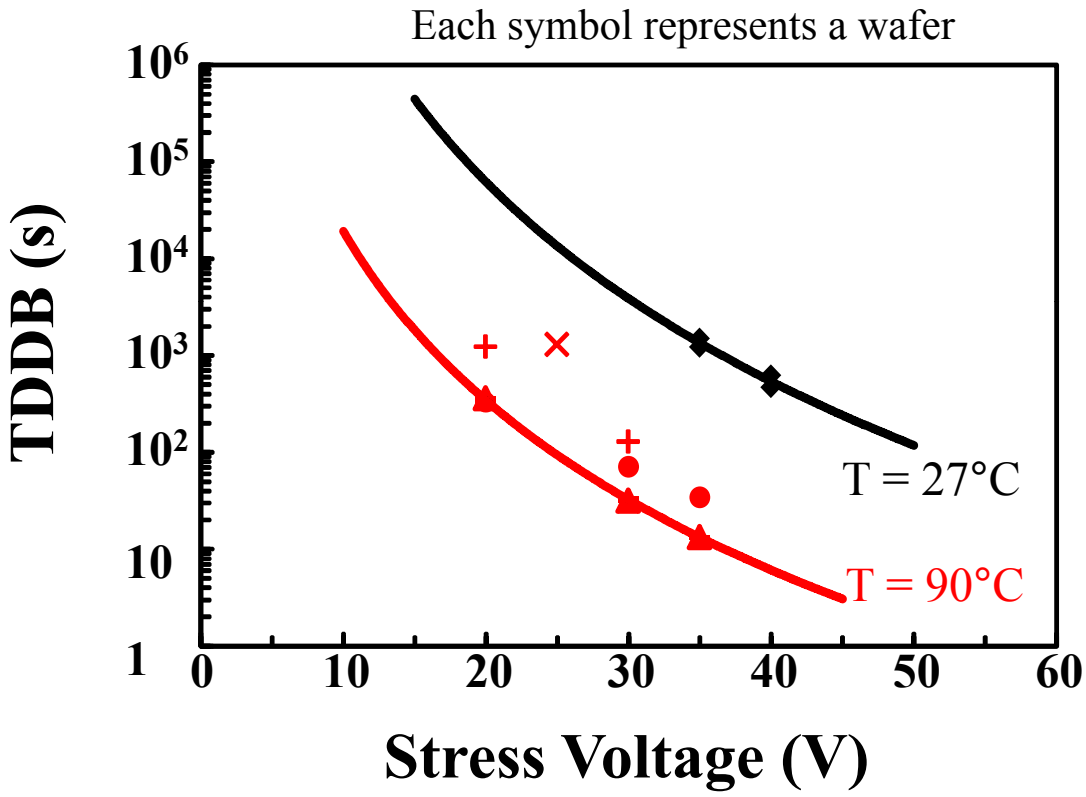
Time to breakdown : voltage acceleration





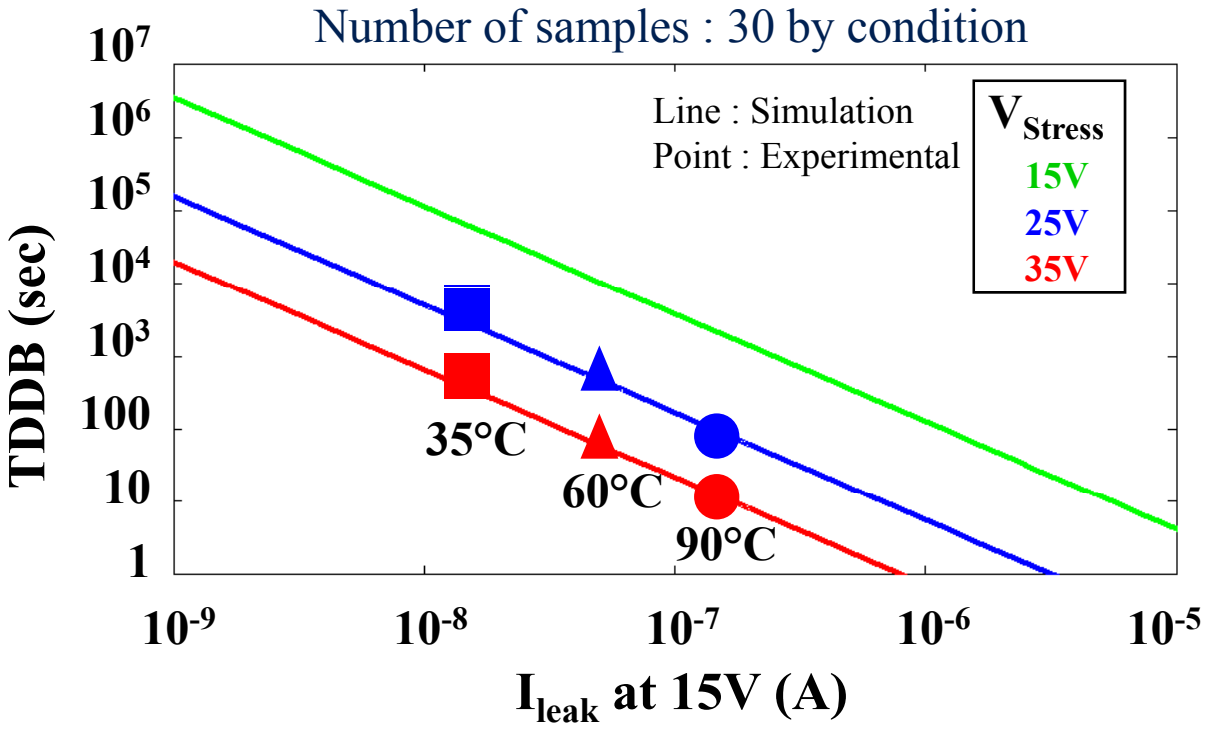
- TDDB experimental values follows a power law : TDDB ~V^{-n}

Time to breakdown modelling 1/2



- For same stress condition, TDDB may be **wafer dependent**
  - Dependence on different initial leakage level

Time to breakdown modelling 2/2



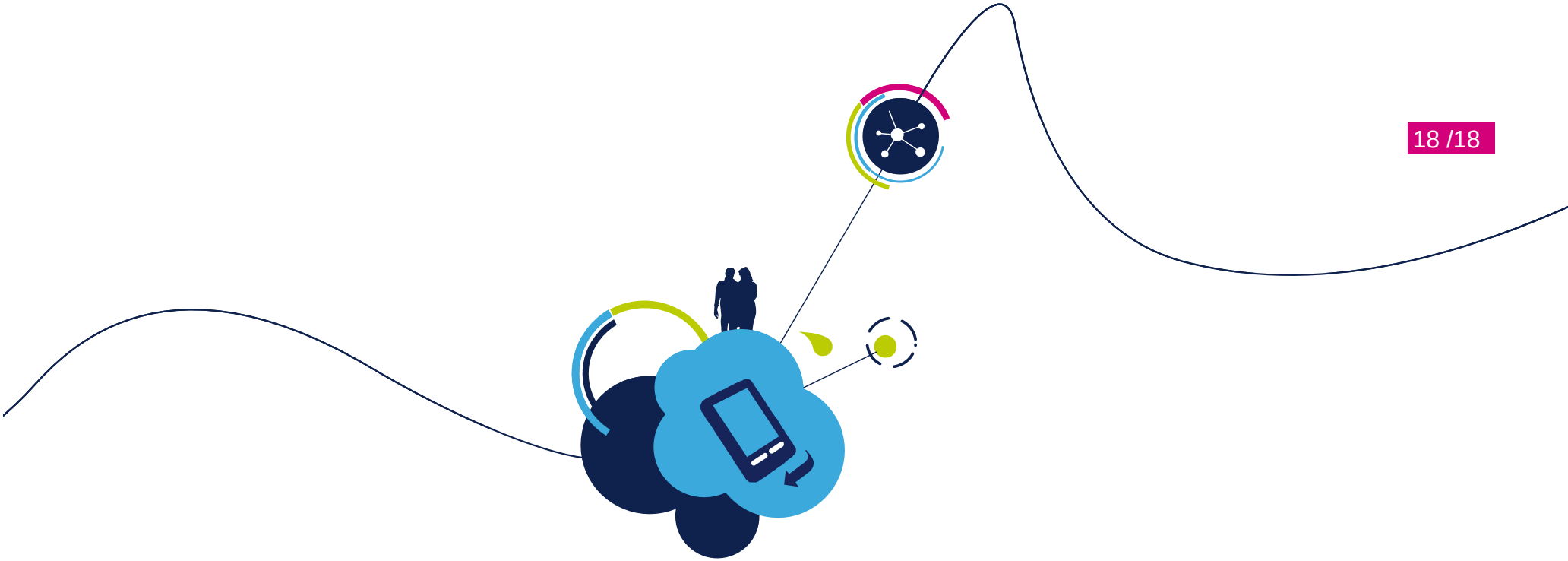
$$TDDB = A \times (I_{leak} \text{ at } 15V)^{-p}$$
$$\text{with } A = \alpha \times V_{stress}{}^{-n}$$

- A: voltage acceleration factor
- $I_{leak} \approx I_{PF}$ which depends on T°, V_{stress}

- TDDB depends on initial leakage current

Conclusion

- Electrical characterization
  - Bake impact
  - Leakage current annealing at high temperature
  - Leakage current kinetic at room temperature
- Modelling
  - Leakage current simulation
  - Time to breakdown modelling
- Forecast
  - TDDB modelling taking into account the annealing phenomenon
  - Ions movement at high temperature and room temperature
  - Ions species



Thank you for your attention.

Some questions ?

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