Full-band simulation of p-type ultra-scaled silicon nanowire transistors

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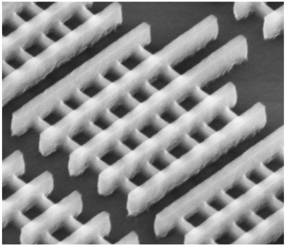
Outline

Nanowire FETs



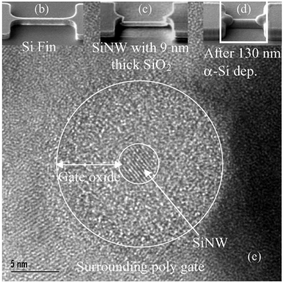
http://www.intel.com/technology/architecture-silicon/22nm

FinFET (Intel, 2011): 3-D tri-gate structure.

- Better electrostatic control than in planar devices.
- Less leakage current.
- Steeper subthreshold slope.
- Higher ON-current.

What is next? Natural evolution of FinFETs towards ultra-scaled, circular, gate-all-around nanowires (NWFETs with $d = 3$ nm already exist).

Computer simulations can accelerate the transistors' evolution (selecting the adequate materials, structural parameters...).



N. Singh et al. IEEE Electron Device Letters, vol. 27, no. 5 p. 383 (2006)

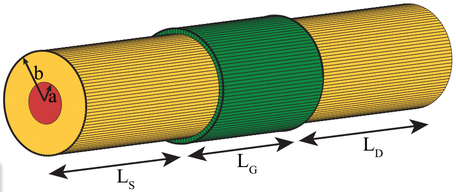
State of computational research

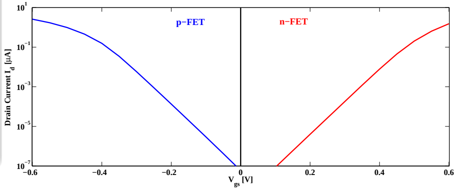
3-D full band quantum transport simulations are the most advanced techniques.

Typical full-band approach (OMEN)

- Empirical tight-binding model.
- Atomistic description.
- Parallelization of the workload.
- Heavy computational burden!

Need for simpler, faster simulation methods to rapidly explore large design spaces.





NEGF:

$$(E - H - \Sigma)\, G^R = I$$

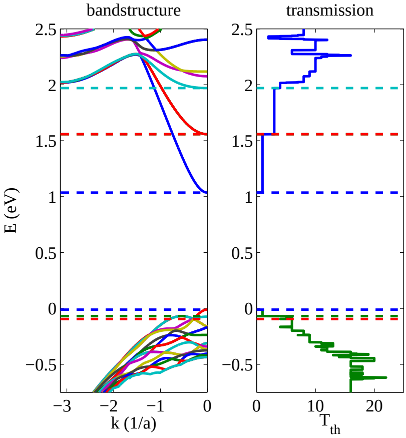
$$size(H) = (N_A \cdot tb) \times (N_A \cdot tb)$$

Outline

Top of the Barrier (ToB) model

Landauer-Büttiker formalism in 1-D

$$I_D = -\frac{q}{\hbar}\int_{-\infty}^{\infty}\frac{dE}{2\pi}T(E)\left(f_S(E)-f_D(E)\right)$$



- Ballistic transport.
- Transmission T(E) = number of available bands at energy E.
- Transistor physics is reduced to a single point, the top/bottom of the electrostatic potential barrier (ToB).
- Works well for NWFETs with $L_G > 15$ nm.

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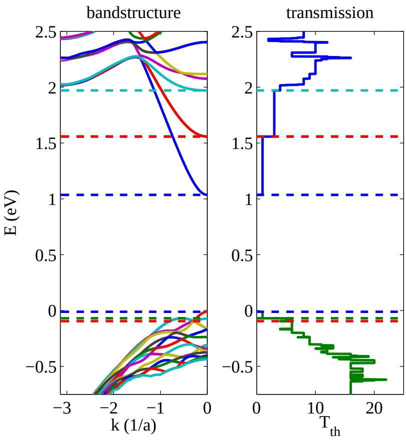

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- Works well for NWFETs with $L_G > 15$ nm.

Fails to describe source-to-drain tunneling in short-channel devices!

Goals

Goal: Determine the I-V characteristics of devices with $L_G < 10$ nm, where intra-band tunneling is significant.

Total drain current (Landauer-Büttiker)

$I_D =$ thermionic current $(I_{th}) +$ tunneling current (I_{tun})

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Quantities to be determined first:

- charge-density
- electrostatic potential

ToB picture: $\rho(V(x))$
Poisson: $V(\rho(x))$
self-consistently

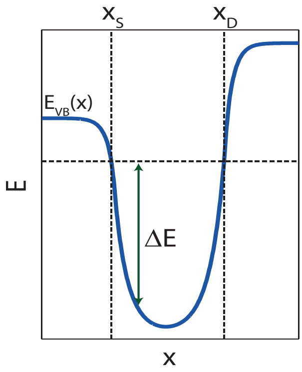
Then I_{tun} can be calculated using the WKB approximation.

Wentzel-Kramers-Brillouin approximation

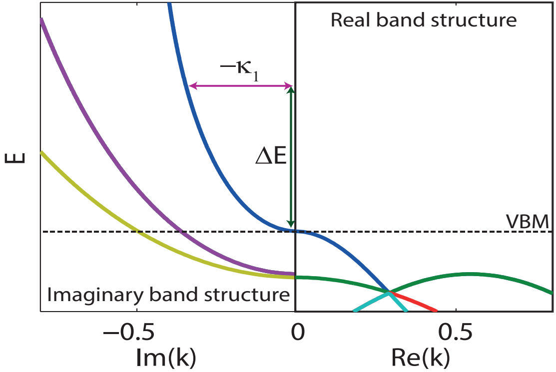
WKB transmission through the barrier

$$T_{WKB}(E) = \sum_n \exp\left(-2\int_{x_{n,S}(E)}^{x_{n,D}(E)} \kappa_n(x)dx\right)$$

Electrostatic potential

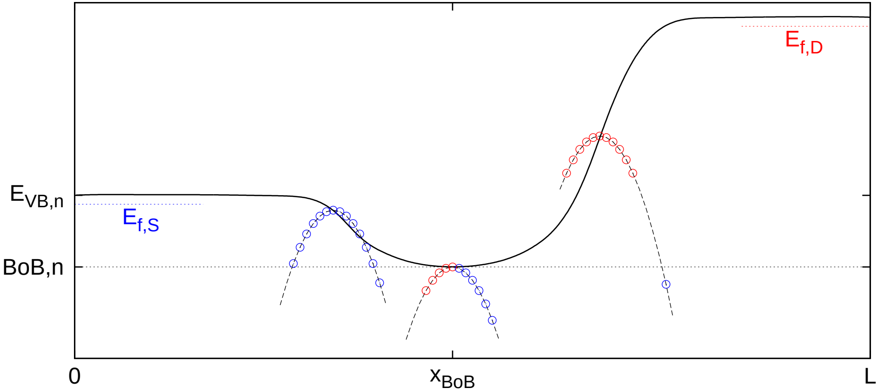


Band structure



Charge density calculation

- Band structure is shifted with the electrostatic potential.
- Electron states are filled with respect to the S/D Fermi levels, considering reflection from the barrier.



Modified Poisson-equation

Poisson-equation in 3-D

$$\Delta\Phi(x,y,z) = -\frac{\rho(x)}{\varepsilon_0\varepsilon_{\mathrm{sc}}}$$

Simplifications:

- Cylindrical symmetry.
- Separation of variables.
- Parabolic approximation in the channel.
- Gate oxide acts like an ideal coaxial capacitor.
- Potential decays exponentially in the oxide around the source/drain extensions.

1-D Poisson-equation in the gate region

$$\frac{d^2\Phi(x)}{dx^2} + \frac{\Phi_g - \Phi(x)}{\lambda^2} = -\frac{\rho(x)}{\varepsilon_0\varepsilon_{\mathrm{sc}}}$$

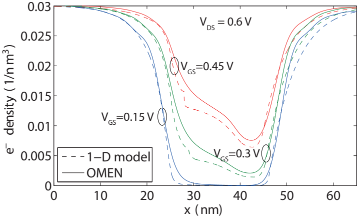
Outline

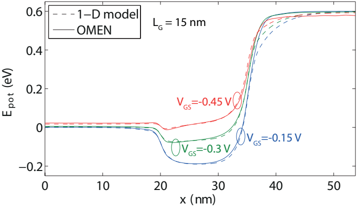
1. Motivation
2. Simulation approach
3. Model validation
4. Investigation of p-type NWFETs
5. Summary

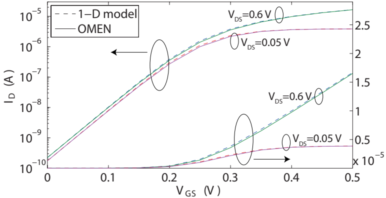
Comparison with 3-D atomistic simulations

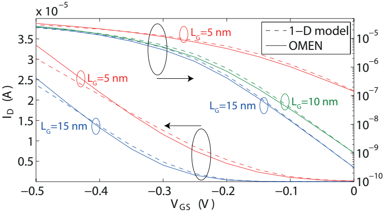
- n-InAs<100>
- $d = 4$ nm
- $L_G = 15$ nm

- p-Si<110> with 1 % strain
- $d = 4$ nm
- $L_G = \{5, 10, 15\}$ nm









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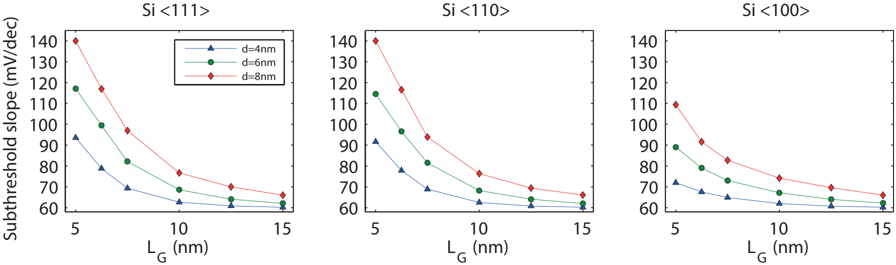
Subthreshold slopes

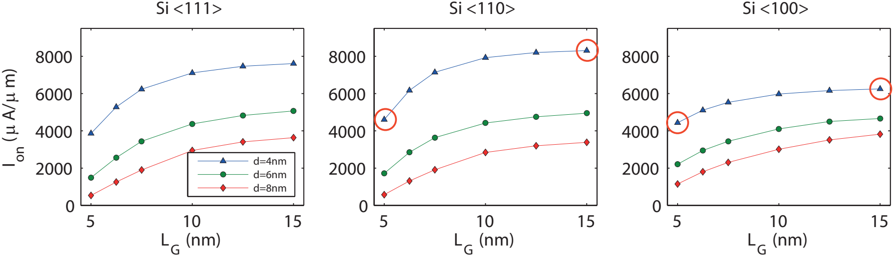


$d = 4$ nm

orientation	m^* $[m_0]$	$\kappa_1(0.2)$ [1/nm]
<111>	0.12	0.76
<110>	0.14	0.81
<100>	0.49	1.28

- Low m_{eff} $\rightarrow$ low κ, high tunneling rate.
- At short gate lengths source-to-drain tunneling limits the performance.

Normalized ON-state currents ($I_{off} = 0.1\mu A/\mu m$)



- Low m_{eff} $\rightarrow$ high I_{on} at large gate lengths (high injection velocity).
- Low κ $\rightarrow$ increased tunneling rate, lower I_{on}/I_{off} ratio at short gate lengths.
- Good compromise is needed with m^* and κ.
- High mobility may become disadvantageous (m_{eff} and κ are not independent).
- Small diameter ($d < 5$ nm) is crucial when $L_G < 10$ nm (better electrostatic control).

Outline

Summary

- Fast and accurate simulator was developed, based on the ToB model and accounting for intra-band tunneling through the WKB approximation.
- The model works well for both n- and p-type NWFETs.
- Gate-all-around nanowires with a wide range of design parameters were investigated.
- Low effective mass usually results in higher tunneling rates at short gate lengths.
- Small channel diameter (<5 nm) is needed when $L_G < 10$ nm.