



## IMPACT OF $\text{Al}_2\text{O}_3$ POSITION ON PERFORMANCES AND RELIABILITY IN HIGH-K METAL GATED DRAM PERIPHERY TRANSISTORS

**M. AOULAICHE<sup>1</sup>, A. FEDERICO<sup>2</sup>, E. SIMOEN<sup>1</sup>, R. RITZENTHALER<sup>1</sup>, T. SCHRAM<sup>1</sup>,  
H. ARIMURA<sup>1</sup>, M. CHO<sup>1</sup>, T. KAUERAUF<sup>1</sup>, F. CRUPI<sup>2</sup>, A. SPESSOT<sup>3</sup>, C. CAILLAT<sup>3</sup>, P. FAZAN<sup>3</sup>,  
H.-J. NA<sup>4</sup>, Y. SON<sup>5</sup>, K. B. NOH<sup>5</sup>, G. GROESENEKEN<sup>1\*</sup>, N. Horiguchi<sup>1</sup>, A. THEAN<sup>1</sup>.**

1. Imec, Kapeldreef 75, 3001 Leuven, Belgium.

\*also with KU Leuven.

2. University of Calabria.

3. Micron Technology Belgium, imec Campus.

4. Samsung Electronics assignee at imec.

5. SK-Hynix assignee at imec.



# OUTLINE

- I. Introduction
- II. Samples description
- III. Performances
- IV. Defects characterization (noise and CP)
- V. Reliability (NBTI)
- VI. Conclusions

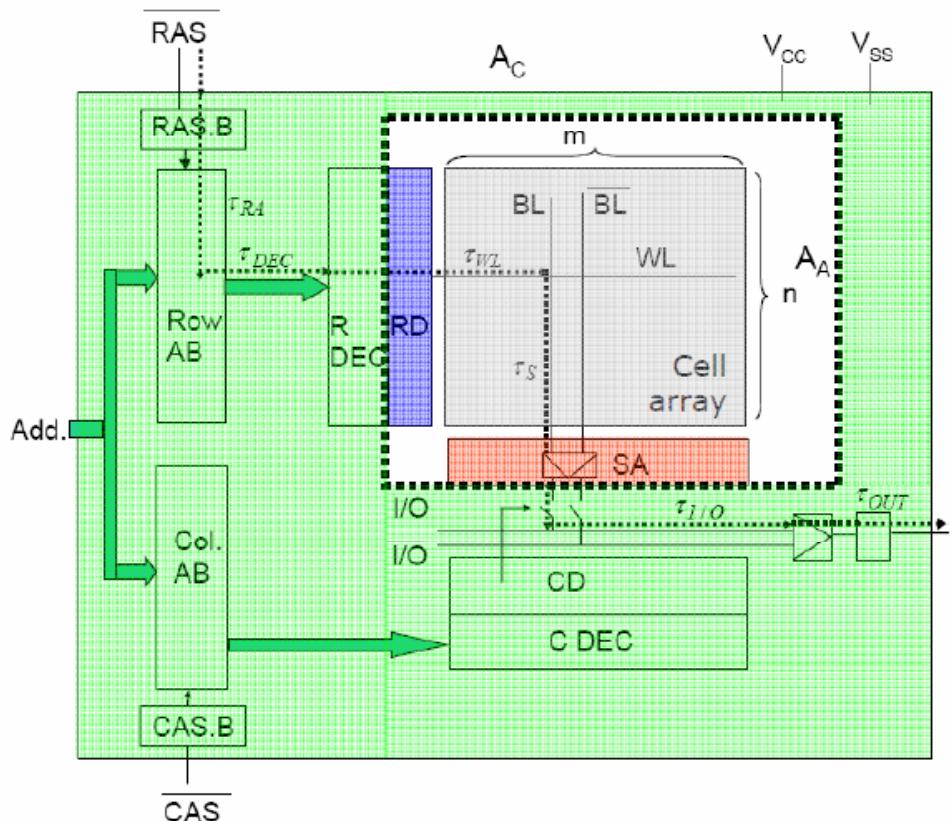
# INTRODUCTION

✓ **DRAM “periphery transistors”:**  
MOSFET used in the DRAM peripheral  
circuitry e.g.

- **Sense amplifiers**
- **Address decoders,**
- **High voltage applications**

✓ **DRAM “periphery transistors”**  
are formed before the DRAM cell  
process.

Therefore they experience the high  
thermal budget related the DRAM cell  
process.



source: S.Y. Cha, "DRAM Technology - History & Challenges" @ IEDM 2011 short courses for more details

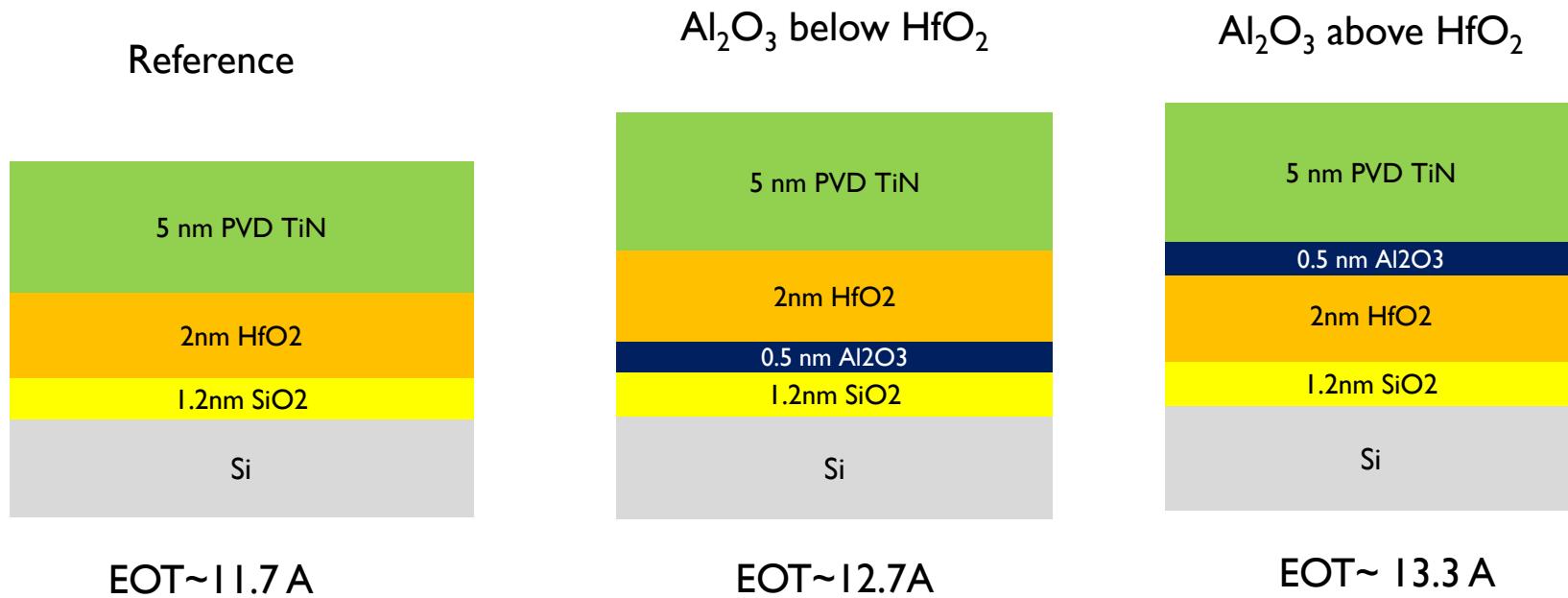
# INTRODUCTION

- Compared to logic applications, DRAM Periphery devices have more relaxed device specifications ( $L_G$ , EOT)
- Required **performance similar to that of logic transistors**, but with a number of additional challenges to be tackled: **low power low leakages** (low  $I_{OFF}$  and  $J_G$  mandatory)
- **HKMG** is needed for future technologies to sustain the performance
  - Stacks surviving the **aggressive anneal** needed in a DRAM process (before silicidation, typically several hours above 600C)

Ref: S.Y. Cha, "DRAM Technology - History & Challenges" @ IEDM 2011 short courses for more details

- I. Introduction
- II. Samples description**
- III. Performances
- IV. Defects characterization (noise and CP)
- V. Reliability (NBTI)
- VI. Conclusions

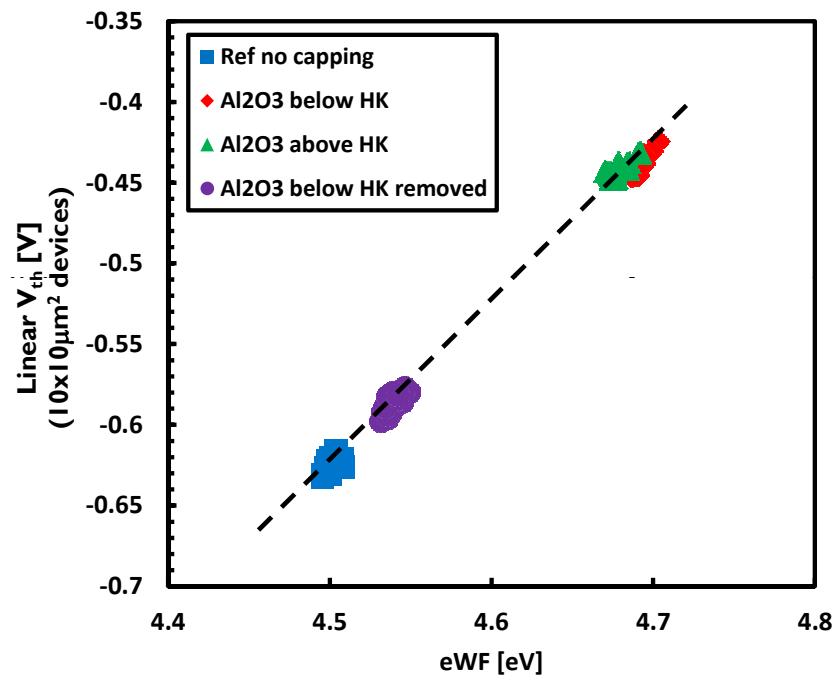
# INVESTIGATED SAMPLES



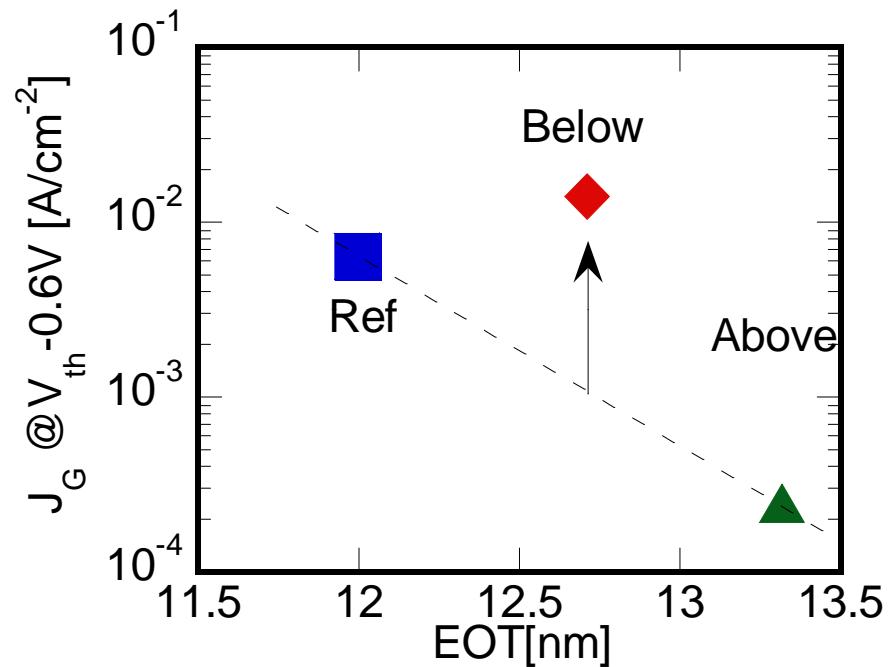
$\text{Al}_2\text{O}_3$  capping is used in pMOSFETs for  $V_{th}$  adjustment

- I. Introduction
- II. Samples description
- III. Performances**
- IV. Defects characterization (noise and CP)
- V. Reliability (NBTI)
- VI. Conclusions

# THRESHOLD VOLTAGE SHIFT AND LEAKAGE

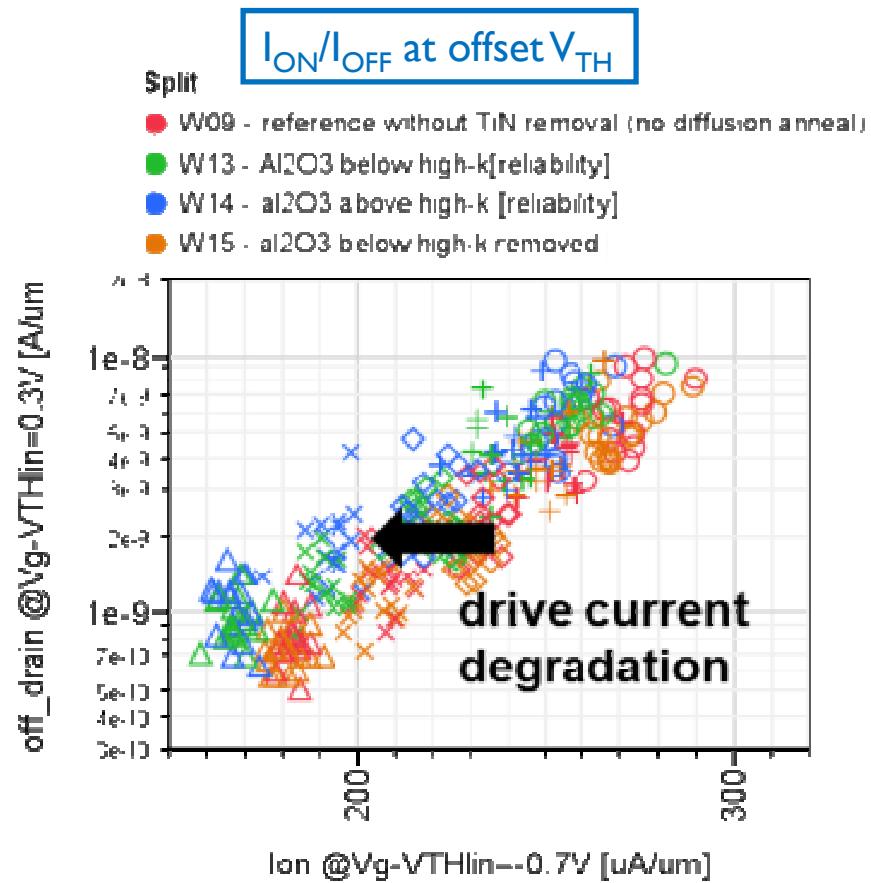
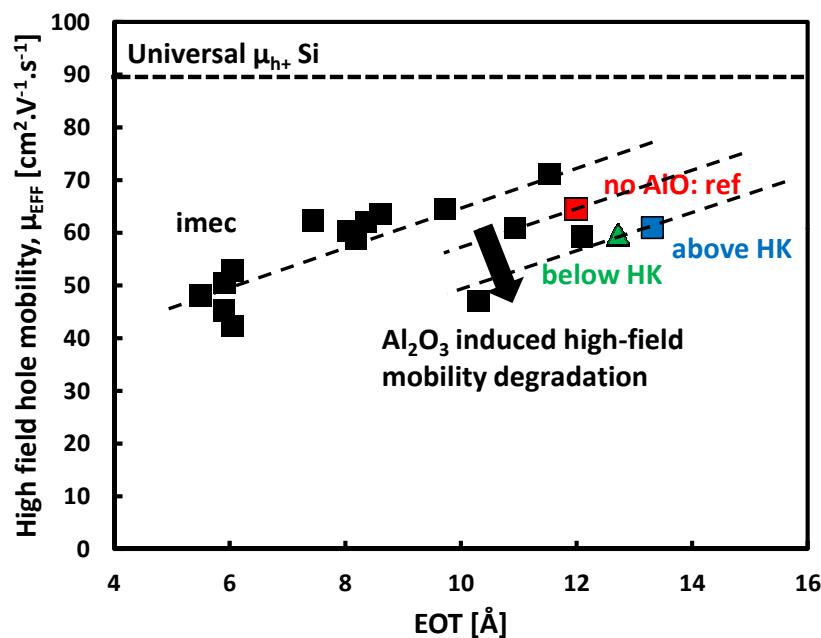


~200mV  $V_{th}$  shift using Al<sub>2</sub>O<sub>3</sub> independently of the capping location.



Lower EOT and higher  $J_G$  for Al<sub>2</sub>O<sub>3</sub> below HfO<sub>2</sub>.  
→ Probably intermixing with the SiO<sub>2</sub> interfacial layer and K value change and Si/SiO<sub>2</sub> energy offset change.

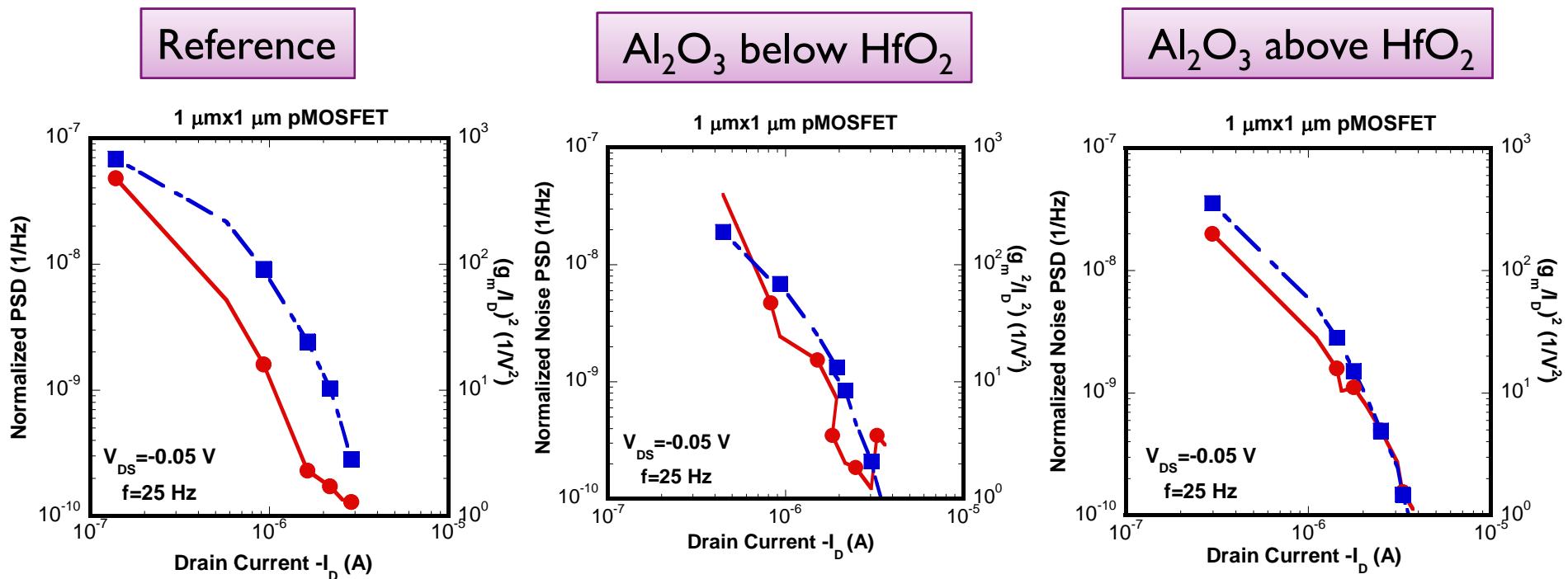
# PERFORMANCES



- Higher EOT and lower mobility translate into lower ON current at fixed  $V_{\text{TH}}$  (trade-off between mobility and  $V_{\text{TH}}$  shift)
- No difference for capping above or below high-k

- I. Introduction
- II. Samples description
- III. Performances
- IV. Defects characterization (noise and CP)**
- V. Reliability (NBTI)
- VI. Conclusions

# LOW FREQUENCY NOISE



LF noise is dominated by number fluctuations  
– i.e., trapping in the gate oxide.

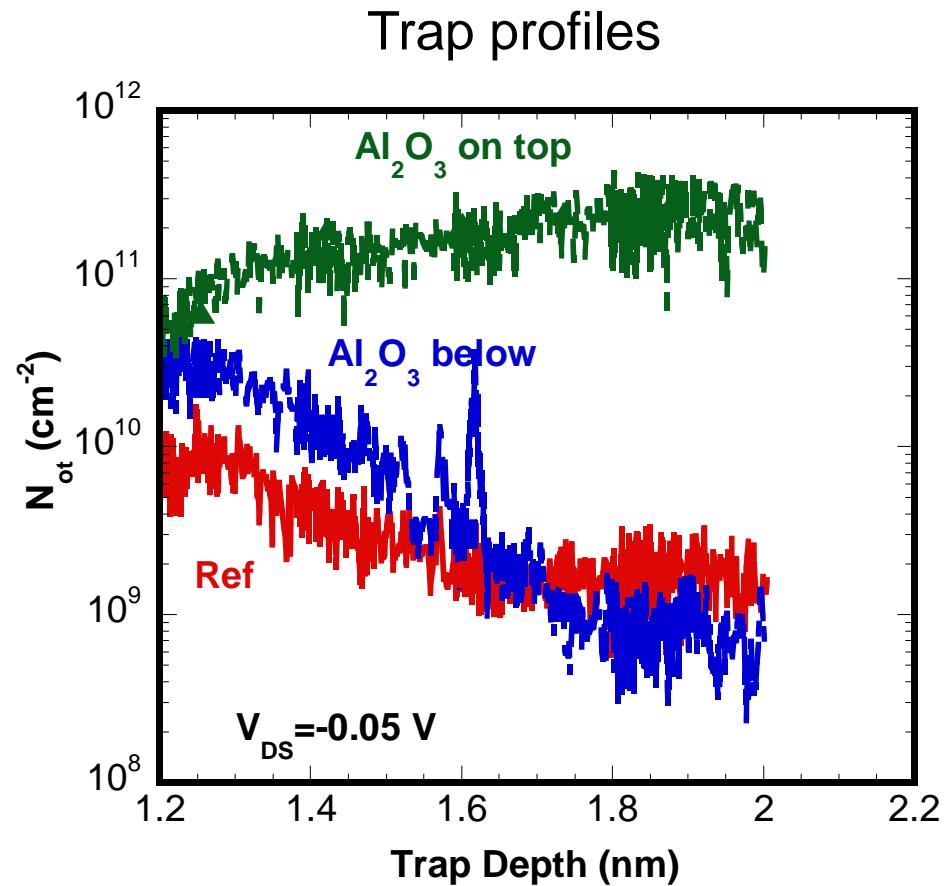
# LOW FREQUENCY NOISE

$$S_{VG} = \frac{q^2 k T N_{ot}}{WLC_{EOT}^2 \alpha_t f}$$



$$N_{ot} = \frac{S_{VG} WLC_{EOT}^2 \alpha_t f}{q^2 K_B T}$$

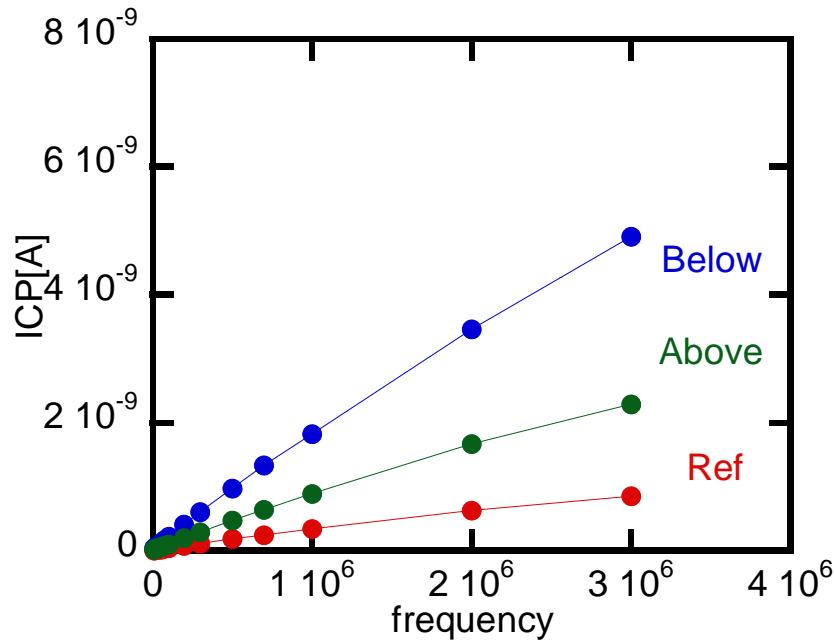
$$z = \frac{\hbar}{2\sqrt{2.q.m_{ox}\phi_{it}}} \ln\left(\frac{1}{2\pi f\tau_0}\right)$$



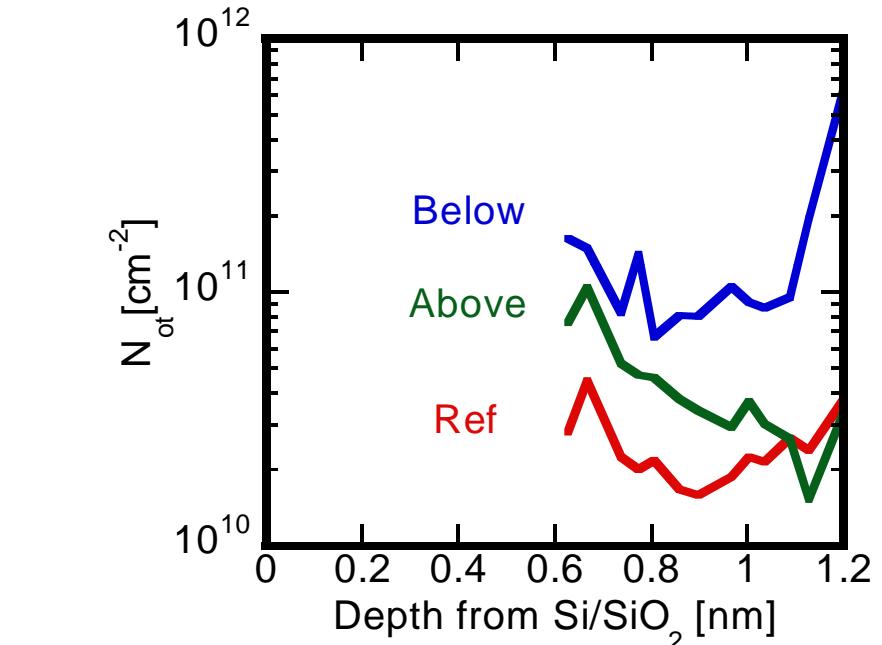
The trap profiles close to the valence band seem to be more sensitive to the additional cap layers.

- [1] G. Ghibaudo, et al. "Improved analysis of low frequency noise in field-effect MOS transistors," *phys. stat. sol. (a)*, vol. 174, pp. 571-581, 1991.
- [2] E. Simoen , et al. "On the flicker noise in submicron silicon MOSFETs," *Solid-St. Electron.*, vol. 43, no. 5, pp. 865-882, May 1999.
- [3] Z. Çelik and T.Y. Hsiang, "Study of 1/f noise in N-MOSFET's: Linear region," *IEEE Trans. Electron Devices*, vol. 32, no. 12, pp. 2797-2802, Dec. 1985
- [27] F.P. Heiman et al. "The effects of oxide traps on the MOS capacitance," *IEEE Trans. Electron Devices*, vol. ED-12, pp. 167-178, Apr. 1965.
- [28] I. Lundström et al., "Tunneling to traps in insulators," *J. Appl. Phys.*, vol. 43, no. 12, pp. 5045-5047, Dec. 1972.

# VARIABLE FREQUENCY CHARGE PUMPING CURRENT



$$Not = \frac{dQ_{cy}}{d \log(f)}$$

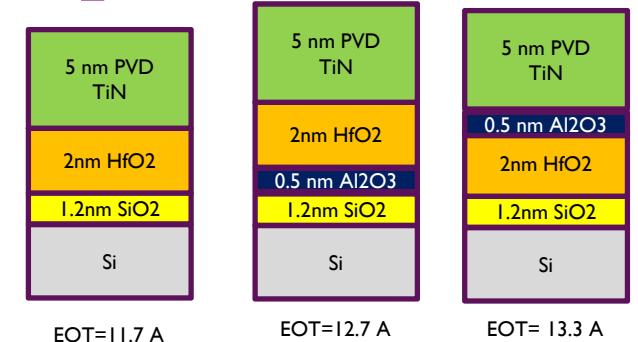
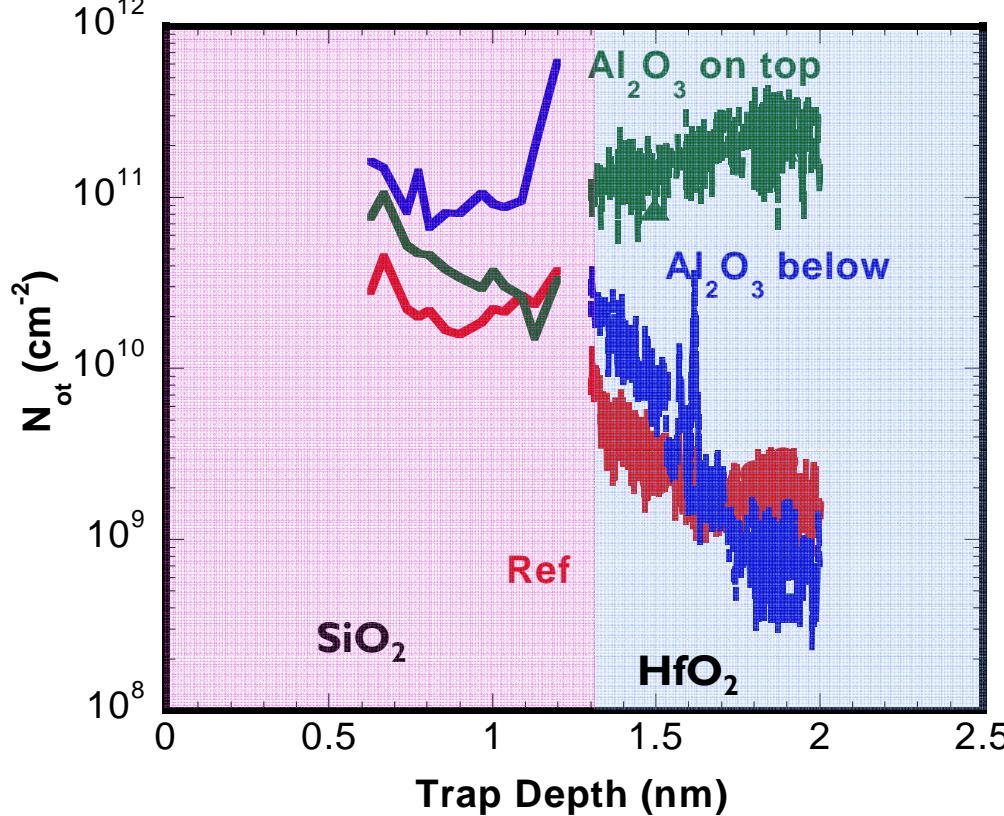


$$\text{and } z = \frac{\hbar}{2\sqrt{2.q.m_{ox}\phi_{it}}} \ln\left(\frac{1}{2\pi f\tau_0}\right)$$

A slightly higher defects density in the  $\text{SiO}_2$  interfacial layer for  $\text{Al}_2\text{O}_3$  below  $\text{HfO}_2$

M.Cho et al.“Study of the Reliability Impact of Chlorine Precursor Residues in Thin Atomic-Layer-Deposited  $\text{HfO}_2$  Layers” IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 4, 2007

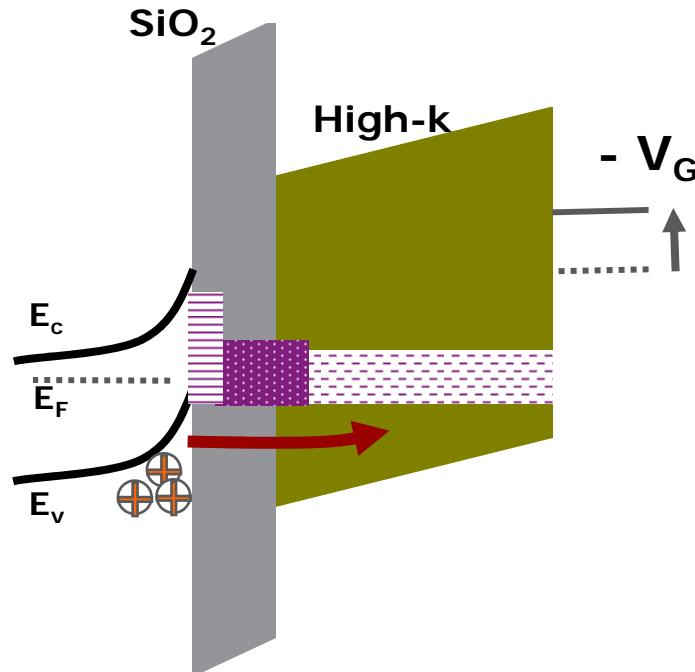
# IMPACT OF $\text{Al}_2\text{O}_3$ LOCATION: BOTTOM OR TOP OF $\text{HfO}_2$



Trap profile follows the expected Al diffusion

- I. Introduction
- II. Samples description
- III. Performances
- IV. Defects characterization (noise and CP)
- V. Reliability (NBTI)
- VI. Conclusions

# NBTI IN DRAM PERIPHERAL DEVICES



- Interface defects and bulk defects induce a  $V_{th}$  shift during the stress.
- $\Delta V_{th}$  kinetics obeys a power law time dependence on  $V_G$ ,  $E_{ox}$ , EOT ( $t_{ox}$ )
- Thermally activated
- Bulk defects impact on the  $\Delta V_{th}$  kinetics.
- Device lifetime is extrapolated for a given  $\Delta V_{th}$  (design specifications)

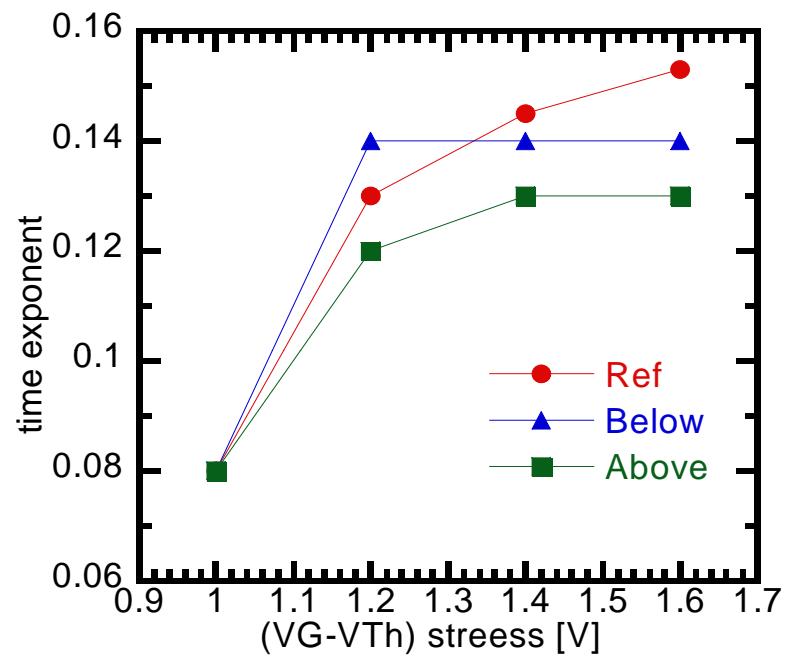
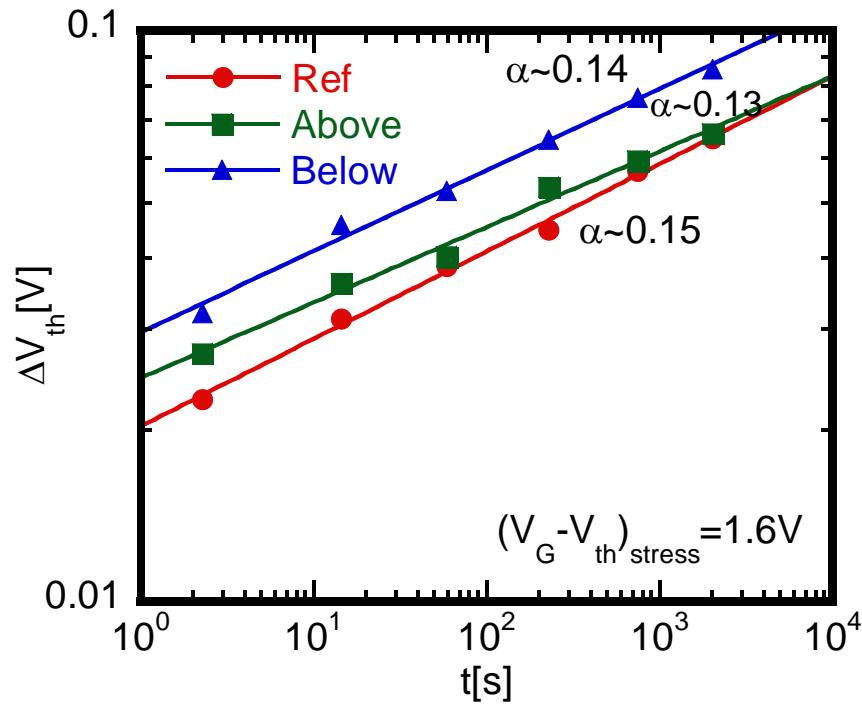
$$\Delta V_{th}(t, V_G, EOT, T) = C \cdot \exp\left(\frac{-Ea}{kT}\right) \left(\frac{V_G - V_{th}}{EOT}\right)^m \cdot t^\alpha$$

temperature

Related to the stack

Field

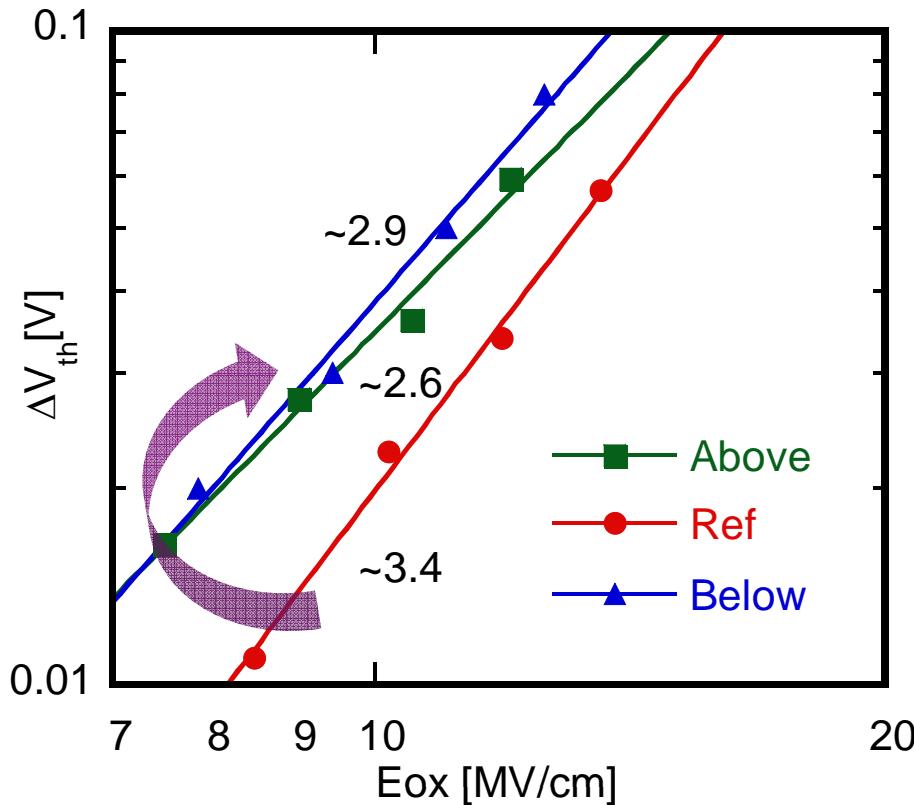
# $\Delta V_{th}$ VERSUS STRESS TIME



$$\Delta V_{th}(t) = C \cdot \left( \frac{V_G - V_{th}}{EOT} \right)^m \cdot t^\alpha$$

Higher density of bulk defects lower time exponent

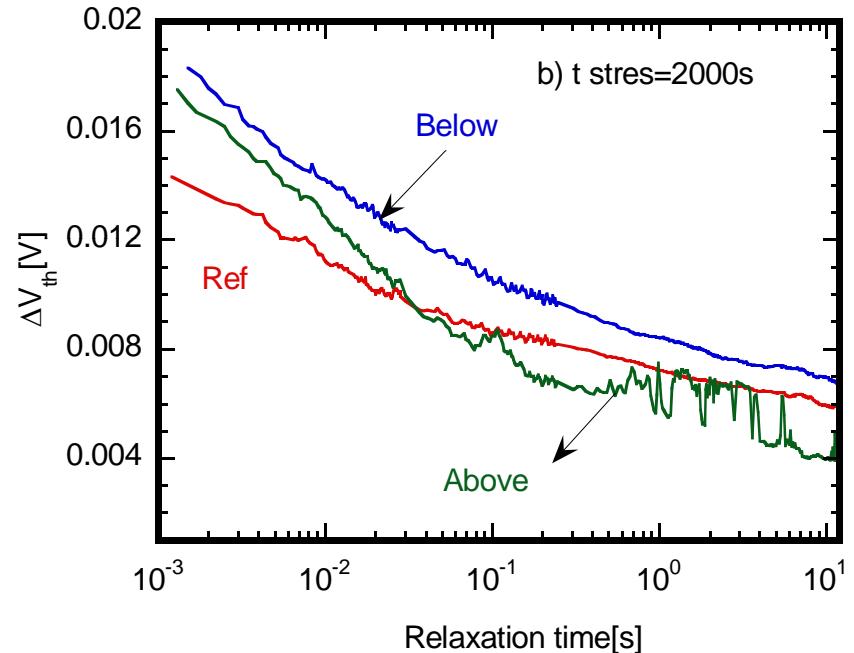
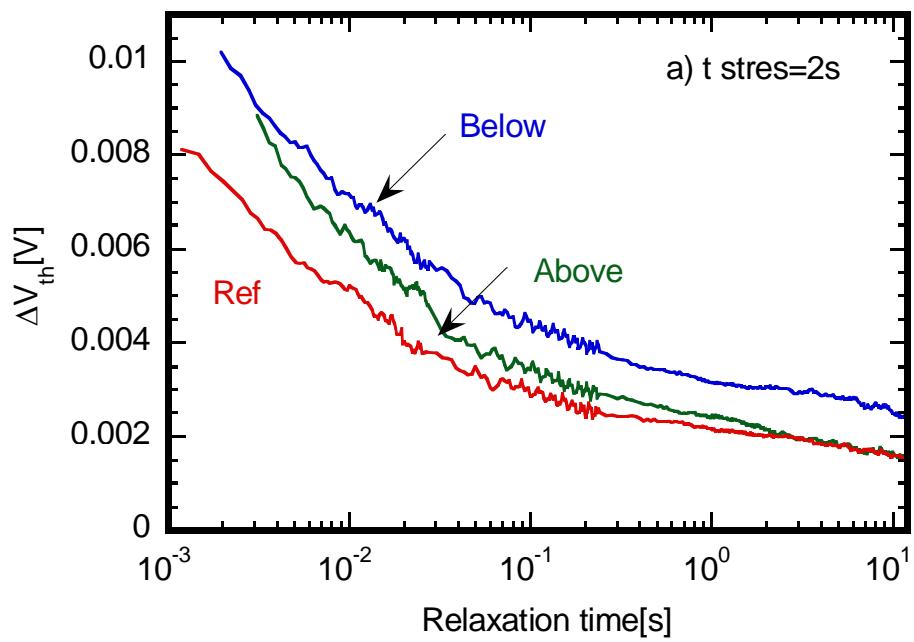
# FIELD ACCELERATION



$$\Delta V_{th}(E_{ox}) = C \cdot E_{ox}^m \cdot t^\alpha$$

More bulk defects higher degradation at lower field and lower field exponent and lower field exponent

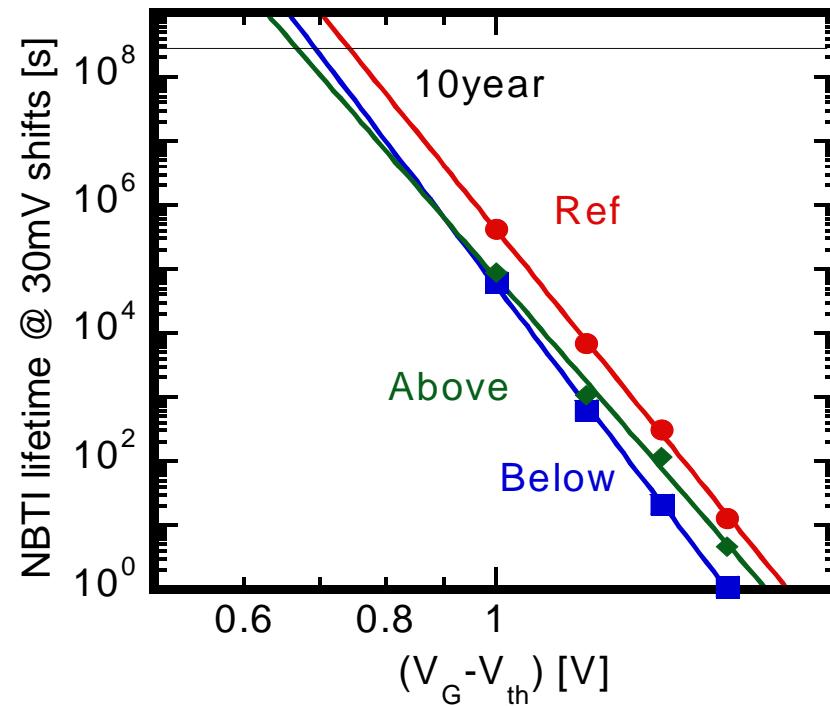
# $\Delta V_{th}$ RELAXATION



- Faster  $V_{th}$  recovery for  $\text{Al}_2\text{O}_3$  above  $\text{HfO}_2$
- Relaxation for  $t > 1\text{ ms}$  is more sensitive to slow traps (farther from the interface)

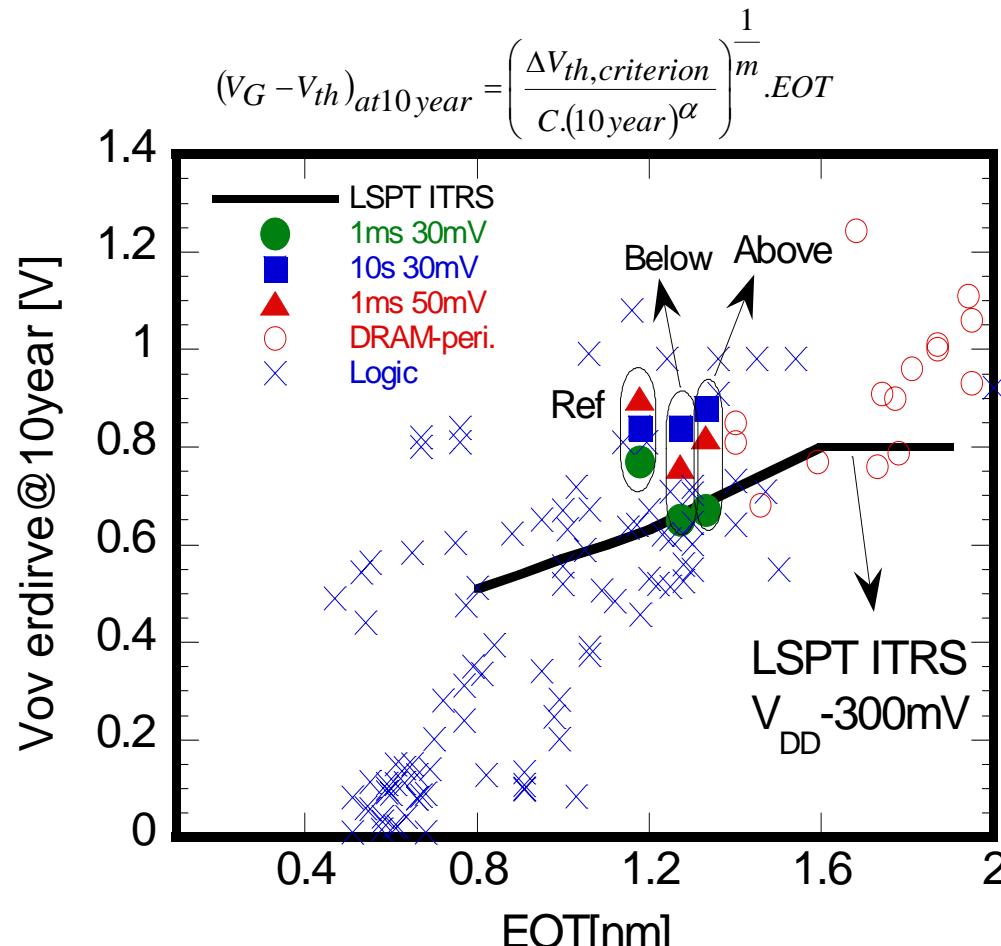
# NBTI LIFETIME EXTRAPOLATION

$$Time\ to\ failure = \left( \frac{\Delta V_{th,criterion}}{C} \right)^{\frac{1}{\alpha}} \cdot (EOT)^{\frac{m}{\alpha}} \cdot \left( \frac{1}{V_G - V_{th}} \right)^{\frac{m}{\alpha}}$$



NBTI is slightly degraded when  $\text{Al}_2\text{O}_3$  is incorporated either below or above  $\text{HfO}_2$

# NBTI LIFETIME EXTRAPOLATION



NBTI is slightly degraded when  $\text{Al}_2\text{O}_3$  is incorporated either below or above  $\text{HfO}_2$

M. Cho, J-D. Lee, M. Aoulaiche, B. Kaczer, Ph.J. Roussel, T. Kauerauf, R. Degraeve, J. Franco, L.-Å. Ragnarsson, and G. Groeseneken, "Insight Into N/PBTI Mechanisms in Sub-1-nm-EOT Devices", IEEE Trans. On Elect. Dev., vol. 59, No. 8, pp.2042-2048, 2012.

- I. Introduction
- II. Samples description
- III. Performances
- IV. Defects characterization (noise and CP)
- V. Reliability (NBTI)
- VI. Conclusions

# CONCLUSIONS

- The defect density profiles from the low frequency noise and charge pumping current are in agreement with what can be expected from traps related to Al diffusion.  
→ The higher peak density of traps is at the location where the  $\text{Al}_2\text{O}_3$  cap is inserted.
- Increased leakage current and reduced LF noise for  $\text{Al}_2\text{O}_3$  below  $\text{HfO}_2$ .
- NBTI is slightly degraded when  $\text{Al}_2\text{O}_3$  is incorporated either below or on top of  $\text{HfO}_2$  compared to the reference.



# Thank you

ASPIRE  
INVENT  
ACHIEVE



GLOBALFOUNDRIES



Panasonic  
ideas for life



ELPIDA



TOSHIBA  
SanDisk

SONY

FUJITSU

QUALCOMM