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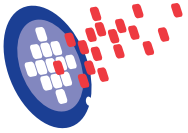


On behalf of the Organizing Committees of ESSDERC 2013, it is our pleasure to welcome you to the 43rd European Solid-State Device Research Conference. ESSDERC 2013 runs in parallel to its sister conference ESSCIRC 2013, covering all aspects of modern solid-state systems, circuits and devices at a single event. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts and circuits and system designers. As a participant at ESSDERC and ESSCIRC, you will have the opportunity to learn of the latest advances in these fields, and to meet those who have dared, pioneered and succeeded.

The conferences are to be held at the JW Marriott Bucharest Grand Hotel, conveniently situated downtown. The venue is located next to the Parliament Palace, the largest building in Europe and the second largest in the world, right after the Pentagon.

This year, a total of 150 submissions originating from 25 countries were received for ESSDERC including 109 papers coming from Europe, 28 from Asia-Pacific, 2 from Middle East and 11 from North-America. This is a proof of the truly international nature of ESSDERC. The Technical Program Committee with 95 world-class experts from academia and industry selected 74 papers for oral presentations. Six sessions with invited papers have been brought in with especially two joint ESSDERC/ESSCIRC sessions: the first one is dedicated to compact modeling; the second is dedicated to reliability and variability. Twelve plenary presentations (six of them suggested by ESSDERC) by outstanding guest speakers complete the program by focusing on highly relevant topics selected by the Technical Program Committees of both conferences.

In addition to the conference programs, a pre-conference day with introductory tutorials and a post-conference day with workshops showcasing work currently being carried out by European research consortia will also be held.

For this year edition, we are honored to host a round table on "The Future of Semiconductor Industry in Europe" with the participation of high level representatives of the major microelectronic companies, research institutes, as well as the funding organizations in Europe. The round table will offer the

panelists the chance to share their views on the topics that ensure the strength and sustainability of the microelectronic industry in Europe.

A special workshop on semiconductor research state-of-the-art in Eastern Europe will take place in the last day of the conference. The workshop entitled ”Potential of Eastern European countries in Key Enabling Technologies” is intended to expose to the international community the Eastern European achievements and to facilitate new contacts for future collaboration.

We would like to thank the Steering Committee of ESSDERC/ESSCIRC for giving us the opportunity to organize this event.

The conference has been organized by members of the University ”POLITEHNICA” of Bucharest, ”Gheorghe Asachi” Technical University of Iasi, IMT Bucharest (National Institute for R&D in Microtechnologies) and Infineon Technologies Romania. We would like to thank the authorities of these institutions for their support and for allowing us to devote part of our time to the organization.

Last but not least, we would like to express our greatest appreciation to all the authors who submitted papers to the conference and to all delegates, tutorial lecturers and plenary speakers who have travelled to Bucharest to interact and share their thoughts during the conference.

Enjoy ESSDERC/ESSCIRC 2013 conference and your visit to Bucharest. We hope to see you all back here more often.

Welcome, Bine ați venit!

Michael Neuhäuser
Conference Chair – ESSDERC/ESSCIRC 2013

Dan Dascalu, Adrian Mihai Ionescu
TPC chairs – ESSDERC 2013

University POLITEHNICA of Bucharest is the largest and the oldest technical university in the country and among the most prestigious universities in Romania. The tradition of this institution, developed in over 190 years through the effort of the most important nation's schoolmasters and of the generations of students, is not the only convincing reason. Today, the POLITEHNICA University of Bucharest is undergoing a continuous modernization process, being involved in a permanent dialogue with great universities in Europe and all over the world.

The Technical University „Gheorghe Asachi" Iaşi is among the oldest and prestigious academic institutions in Romania. It has a distinguished presence, both national and international, and it trains engineer professionals, able to quickly and efficiently respond to the innovation, research and development demands of the economic agents.

The University has the resources of intelligence and creativity as well as the skills required to generate, disseminate and implement the results of scientific approaches. Institution is working to strengthen a system of quality assurance and academic excellence in teaching and research.

The National Institute for R&D in Microtechnologies - IMT Bucharest, Romania (www.imt.ro) is supervised by the National Ministry of Education.

The field of activities corresponds to micro-nanosystems, micro-nanoelectronics and nanobio-technology. IMT – Bucharest was the first Eastern European institution promoting MST Technologies and a main performer in the region. Its European dimension is confirmed by its participation in the EU Frame Programs FP6 and FP7 (24 projects in ICT and NMP), FP7-related (11 projects: ENIAC-JU, MNT- ERANET, COST) and in national projects (ICT, Materials, Health, Security, Space).

Welcome to ESSDERC 2013

Platinum Sponsor

Infineon Technologies focuses on the three central challenges facing modern society: Energy Efficiency, Mobility and Security and offers semiconductors and system solutions for automotive and industrial electronics and chip card and security applications.

Infineon's products stand out for their reliability, their quality excellence and their innovative and leading-edge technology in analog and mixed signal, RF and power as well as embedded control.

With a global presence, Infineon operates through its subsidiaries in the USA from Milpitas, California, in the Asia-Pacific region from Singapore, and in Japan from Tokyo. In the 2012 fiscal year (ending September 2012), the company reported sales of 3.9 billion Euro.

Contents

ESSDERC Schedule

Monday, September 16th, 2013

Tutorials

09:30	Tutorials start
12:30 – 14:00	Lunch break
17:00	Tutorials end

See pages 39-40 for details.

Tuesday, September 17th, 2013

8:00 Conference Opening

Technical Sessions

8:30	Joint Plenary Lecture
9:20	Plenary Executive Round Table
10:50	Joint Plenary Lecture
11:40	Lunch
13:00	ESSDERC Sessions
14:20	ESSDERC Key Notes
15:20	Coffee Break
15:50	ESSDERC Invited Session I
16:50	ESSDERC Sessions

Welcome Reception

Wednesday, September 18th, 2013

Technical Sessions

8:30	Joint Plenary Lecture
9:25	Joint Plenary Lecture
10:20	Coffee Break
10:50	ESSDERC Key Note
12:30	Lunch
14:00	ESSDERC Sessions
15:00	ESSDERC Sessions
16:00	Coffee Break
16:30	ESSDERC Sessions

Gala Dinner

Thursday, September 19th, 2013

Technical Sessions

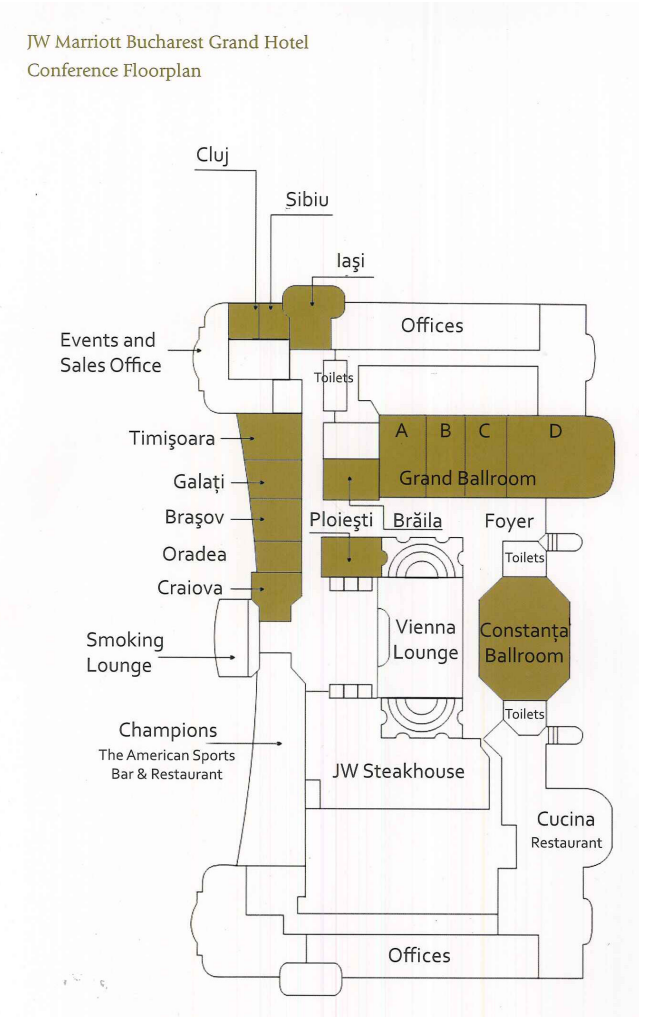
9:00	Joint Plenary Lecture
9:55	Joint Plenary Lecture
10:50	Coffee Break
11:20	ESSDERC Sessions
12:20	Lunch
14:00	ESSDERC Key Note
15:00	ESSDERC Invited II
16:00	Coffee Break
16:20	ESSDERC Sessions

Friday, September 20th, 2013

Workshops

8:50 (9:00)-10:30	Work Session
10:30 – 11:00	Coffee Break
11:00 – 12:00	Work Session
12:00 – 13:30	Lunch
13:30 – 15:00	Work Session
15:00 – 15:30	Coffee Break
15:30 – 18:00	Work Session

Meeting Rooms Floorplan



Tuesday, September 17th, 2013

Time	Room A	Room B	Room C	Room D	Room C T	Room TM
08:00-08:30	**CONFERENCE OPENING** (Michael Neuhäuser, Conference Chair, Rakesh Kumar, IEEE SSCS President) (Room: ABCD)					
08:30-09:20	A1L-A **JOINT PLENARY**: Reinhard Ploss (Infineon) Chr: Michael Neuhaeuser Track: INVITED Joint Plenary (Room: ABCD)					
09:20-10:50	**Round Table: "Europe as Engine of Innovation in the Semiconductor Area"** (Room: ABCD)					
10:50-11:40	A2L-A **JOINT PLENARY**: Witek Maszara (Global Foundries) Chr: Andrei Vladimirescu Track: INVITED Joint Plenary (Room: ABCD)					
11:40-13:00	**Lunch + Exhibition**					
13:00-14:00	A3L-A **Emerging FET Devices** Chr: Radu Sporea, Andreas Schenk Track: ESSDERC-Emerging Non-CMOS Devices & Technologies		A3L-C **GaN and NEMS** Chr: Gunnar Malm, Henryk Przewlocki Track: ESSDERC-Characterization, Reliability & Yield		A3L-E **ESSCIRC Keynote**: E. Candes (Stanford Univ.) Chr: Boris Murmann Track: INVITED ESSCIRC	A3L-F **Emerging FET-like Modeling** Chr: Bernd Meinerzhagen, Wladek Grabinski Track: ESSDERC-Modeling & Simulation
14:00-15:20		14:20-15:20 A4L-B **Energy-Efficient High-Speed Circuits** Chr: Tobias Gemmeke, Doris Schmitt-Landsiedel Track: ESSCIRC-Digital Circuits	A4L-C **mmWave-to-THz Building Blocks and Systems** Chr: Yann Deval, Baudouin Martineau Track: ESSCIRC-RF & mm Wave		14:20-15:20 A4L-E **ESSDERC Keynote**: Tsunenobu Kimoto (Kyoto Univ.) Chr: Florin Udrea Track: INVITED ESSDERC	
15:20-15:50	**Coffee Break + Exhibition**					
15:50-16:50	A5L-A **PLLs** Chr: Francesco Svelto, Antonio Liscidini Track: ESSCIRC-RF & mm Wave	A5L-B **Innovation in Digital Circuit Architectures** Chr: Hannu Tenhunen, Christian Piguet Track: ESSCIRC-Digital Circuits			A5L-E **ESSDERC Invited Session I** Chr: Gunnar Malm Track: INVITED ESSDERC	
16:50-18:50	A6L-A **Analog I** Chr: Marco Berkhout, Traian Visan Track: ESSCIRC-Analog Circuits	A6L-B **Nyquist Rate ADCs** Chr: Georgi Radulov, George Gielen Track: ESSCIRC-Data Converters	A6L-C **Biomedical Circuits & Systems** Chr: Andreas Demosthenous, Firat Yazicioglu Track: ESSCIRC-Bio-Medical & Bio-Electronic Circuits & Systems	A6L-D **Power Converters and Drivers** Chr: Bernhard Wicht, Michael Mark Track: ESSCIRC-Power Management & Energy Scavenging	A6L-E **Technologies and Devices for RF and Power Applications** Chr: Gaudenzio Meneghesso, Gianmauro Pozzovivo Track: ESSDERC-Microwave & Power Solid State Devices	A6L-F **Optoelectronic and Photonic devices** Chr: Ion Tiginyanu Track: ESSDERC-Optoelectronic & Photonic Devices
20:00-23:00	**Welcome Reception at Hilton**					

Wednesday, September 18th, 2013

Time	Room A	Room B	Room C	Room D	Room C T	Room TM
08:30-09:25	B1L-A **JOINT PLENARY**: Wilfried Haensch (IBM) Chr: Adrian Ionescu Track: INVITED Joint Plenary (Room: ABCD)					
09:25-09:35	**Best Paper Awards ESSCIRC/ESSDERC-2012**					
09:35-10:30	B2L-A **JOINT PLENARY**: Stefan Finkbeiner (Bosch) Chr: Franz Dielacher Track: INVITED Joint Plenary (Room: ABCD)					
10:30-10:50	**Coffee Break + Exhibition**					
10:50-12:30	B3L-A **RF Receivers and Front-ends** Chr: Marc Borremans, Paul Muller Track: ESSCIRC-Wireless & Wireline Communication Circuits & Systems	B3L-B **Memories** Chr: Sylvain Clerc, Ralph Hasholzner Track: ESSCIRC-Processors, Memories & Interfaces	B3L-C **Magnetic, Temperature and Pressure Sensors** Chr: Hanspeter Schmid, Werner Brockherde Track: ESSCIRC-Sensors, Imagers & MEMs	B3L-D **Frequency Synthesis** Chr: Pietro Andreani, Jan Crols Track: ESSCIRC-RF & mm Wave	B3L-E **ESSDERC Keynote**: Livio Baldi (Micron) Chr: Raluca Muller Track: INVITED ESSDERC	
12:30-14:00	**Lunch + Exhibition**					
14:00-15:00	B4L-A **Emerging Devices** Chr: Francois Andrieu, Nadine Collaert Track: ESSDERC-Advanced CMOS Devices	B4L-B **Processing & Integration** Chr: Per-Erik Hellström, Simon Deleonibus Track: ESSDERC-Processing & Integration	B4L-C **Emerging Memories I** Chr: Andrea L. Lacaita, Dimitris Tsoukalas Track: ESSDERC-Advanced & Emerging Memories	B4L-D **Reliability Aspects from Device to Circuit I** Chr: Paolo Pavan Track: ESSDERC-Characterization, Reliability & Yield	B4L-E **ESSCIRC Keynote**: B. Murman (Stanford Univ.) Chr: Andrea Baschirotto Track: INVITED ESSCIRC	
15:00-16:00	B5L-A **Si-based Devices** Chr: Maryline Bawedin Track: ESSDERC-Advanced CMOS Devices	B5L-B **Silicon Doping** Chr: Emmanuel Augendre Track: ESSDERC-Processing & Integration		B5L-D **Reliability Aspects from Device to Circuit II** Chr: Paolo Pavan Track: ESSDERC-Characterization, Reliability & Yield	B5L-E **ESSCIRC Invited Session on Emerging Technology** Chr: Edoardo Charbon Track: INVITED ESSCIRC	
16:00-16:30	**Coffee Break + Exhibition**					
16:30-17:50	B6L-A **Emerging MOS: Variability & Defects** Chr: Tibor Grasser, Ray Hueting Track: ESSDERC-Modeling & Simulation	B6L-B **Nanowire Electronics** Chr: Costin Anghel, Elena Gnani Track: ESSDERC-Emerging Non-CMOS Devices & Technologies	B6L-C **Emerging Memories II** Chr: Kazunari Ishimaru, Olivier Thomas Track: ESSDERC-Advanced & Emerging Memories	B6L-D **Application-specific Processors & Circuits** Chr: Stefan Rusu, Marian Verhelst Track: ESSCIRC-Processors, Memories & Interfaces	B6L-E **RF Transceiver Circuits** Chr: Jussi Ryynanen, Peter Baltus Track: ESSCIRC-RF & mm Wave	B6L-F **CMOS Image Sensors** Chr: Angel Rodriguez-Vazquez, Johannes Solhusvik Track: ESSCIRC-Sensors, Imagers & MEMs
18:00-19:00				**ESSCIRC '14 TPC meeting**	**ESSDERC '14 TPC meeting**	
20:00-24:00	**Gala Dinner** **Invited Speaker C. Bulucea: "Eastern Europe's Semiconductor Technology - Recollections and Projections"**					

Thursday, September 19th, 2013

Time	Room A	Room B	Room C	Room D	Room C T	Room TM
09:00-09:55	C1L-A **JOINT PLENARY**: M. Maharbiz (UC, Berkeley) Chr: Liviu Goras Track: INVITED Joint Plenary (Room: ABCD)					
09:55-10:50	C2L-A **JOINT PLENARY**: J. del Alamo (MIT) Chr: Dan Dascalu Track: INVITED Joint Plenary (Room: ABCD)					
10:50-11:20	**Coffee Break + Exhibition**					
11:20-12:20	C3L-A **More than Moore** Chr: Steve Hall, Ryoichi Ishihara Track: ESSDERC-Emerging Non-CMOS Devices & Technologies	C3L-B **MEMS Devices and Technologies I** Chr: Mart Graef Track: ESSDERC-MEMS, Bio-sensors & Display Technologies		C3L-D **Advanced Characterization of Novel MOS FET Structures** Chr: Henryk Przewlocki, Gunnar Malm Track: ESSDERC-Characterization, Reliability & Yield	C3L-E **ESSCIRC Keynote**: P. Kinget (Columbia Univ.) Chr: Peter Mole Track: INVITED ESSCIRC	
12:20-14:00	**Lunch + Exhibition**					
14:00-15:00	C4L-A **Analog II** Chr: Boris Murmann, Hugo Veenstra Track: ESSCIRC-Analog Circuits	C4L-B **Oversampled ADCs I** Chr: Lucien Breems, Angelo Nagari Track: ESSCIRC-Data Converters	C4L-C **Millimeter-wave Circuits** Chr: Sven Mattisson, Peter Kennedy Track: ESSCIRC-Wireless & Wireline Communication Circuits & Systems	C4L-D **LED/LCD Drivers** Chr: Michiel Steyaert, Philip Mok Track: ESSCIRC-Power Management & Energy Scavenging	C4L-E **ESSDERC Keynote**: Kaustav Banerjee (UC, Santa Barbara) Chr: Max Lemme Track: INVITED ESSDERC	
15:00-16:00	C5L-A **Analog III** Chr: Peter Mole, Willy Sansen Track: ESSCIRC-Analog Circuits	C5L-B **Oversampled** ADCs II Chr: Claudius Dan, Piero Malcovati Track: ESSCIRC-Data Converters	C5L-C **Wake-up Receivers** Chr: Frank Op't Eynde, Jan Craninckx Track: ESSCIRC-Wireless & Wireline Communication Circuits & Systems	C5L-D **Voltage Regulators and Energy Harvesting** Chr: Marc Pastre, Patrick Reynaert Track: ESSCIRC-Power Management & Energy Scavenging	C5L-E **ESSDERC Invited Session II** Chr: Gheorghe Brezeanu Track: INVITED ESSDERC	
16:00-16:20	**Coffee Break + Exhibition**					
16:20-18:00	C6L-A **VCOs and Dividers** Chr: Andrea Bevilacqua, Alexandre Siligaris Track: ESSCIRC-RF & mm Wave	C6L-B **Circuits and Systems in Emerging Technologies** Chr: Eugenio Cantatore, Thierry Taris Track: ESSCIRC-Circuits & Systems in Emerging Technologies		C6L-D **Carbon-based Devices** Chr: Adrian Ionescu, Mircea Dragoman Track: ESSDERC-Carbon-based Devices	C6L-E **Emerging Memory Modeling** Chr: Cristell Maneux, An De Keetsgieter Track: ESSDERC-Modeling & Simulation	C6L-F **MEMS Devices and Technologies II** Chr: Piotr Grabiec Track: ESSDERC-MEMS, Bio-sensors & Display Technologies

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Welcome to Bucharest

The city of Bucharest is the capital of Romania and its most important cultural, business and financial center. A young and dynamic city, Bucharest has an eclectic architecture, which provides a view into its history. A mixture of medieval, neoclassical and Art Nouveau buildings, the city center also boasts recently built contemporary structures such as skyscrapers and office buildings. The city's majestic architecture and the sophistication of its elite earned Bucharest the nickname of "Little Paris" at the beginning of the 20th century.

Bucharest is easily accessible from all major European cities and with only one-stop connections from Asia and the Americas. The city benefits from a modern international airport and an extensive public transport system that is one of the largest in Europe.

Romania is the largest country in southeastern Europe and a member of the European Union since January 2007. The country is best known worldwide for its beautiful natural landscapes and UNESCO Heritage sites, such as The Danube Delta, the Monasteries of Moldova and the Transylvanian medieval cities. Also known as the mysterious land of the Legend of Dracula, Romania is a whole of fascinating experiences where Authentic, Natural and Cultural are the words that best capture its essence and make up an intriguing country rich in history, arts and scenic beauty.

The conference will be hosted in the upscale JW Marriott Bucharest Grand Hotel conveniently situated downtown. Inaugurated in 2000, the hotel exudes an essence of European elegance and comfort, providing excellent facilities for any large-scale event. The convention center includes 12 reconfigurable rooms adding up to a total of 2044 m2. The hotel is located next to the Parliament Palace, the largest building in Europe and the second largest in the world, right after the Pentagon.

Reaching "JW Marriott Bucharest Grand Hotel" by plane (approximately 1 hour):

When you arrive at Bucharest-Henri Coandă International Airport take the express Line 783 for 16 stations (aprox. 40 min) and get off at "Piața Unirii".

Then take the 385 bus for 6 bus stops (approx. 15 min) and get off at "Piața Arsenalului".

Conference Venue

Reaching "JW Marriott Bucharest Grand Hotel" from Downtown (approximately 30 minutes):

From "Universitate" bus stop (direction "Grădina Cişmigiu") take:

- bus 601, 163, 336 or
- trolleybus 61, 66, 69, 70, 85, 90, 91, 92.

Get off at "Grădina Cişmigiu"

Walk for 5 minutes to the "Elie Radu" bus station (near "Izvor" metro station). Take bus 385.

Stop at "Piaţa Arsenalului"

Language

The official language of the Conference is English

Webpages

ESSCIRC 2013 webpage: esscirc2013.imt.ro
ESSDERC 2013 webpage: essderc2013.imt.ro

Name Badges

All participants and accompanying persons are asked to wear their name badges in a visible place. Entrance to sessions is restricted to registered delegates only. Entrance to meeting halls and exhibition areas are granted to badge holders.

Speakers Briefing

Authors should meet their chairperson in the session room 15 minutes ahead the respective sessions.

Internet Access

Wireless internet access will be available at the conference venue without charge.

Conference Proceedings

All participants will receive an USB stick containing the accepted papers for both ESSCIRC and ESSDERC.

Best Paper Award

Papers presented at the conferences will be considered for the Best Paper Award and for the best “Young Scientist“ Paper Award. The selection will be based on the results of the paper selection process and the judgment of the chairmen. Award delivery will take place at ESSCIRC/ ESSDERC 2014.

Insurance Disclaimer

Participants are responsible for their own insurance. The organizers cannot take responsibility for any accident, loss or damage to participants or their property during the event.

Complaints

While we hope that your time at the conference is enjoyable, if you encounter a problem during your stay, please report it to the registration desk as soon as possible. The conference team will make every effort to rectify the issue.

Conference Overview

The aim of ESSDERC conferences is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. ESSDERC and ESSCIRC (sister conference) are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts and circuits and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC will share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions.

THEMES OF THE CONFERENCE

Advanced CMOS Devices

Ultimate CMOS scaling for high performance, low power and low voltage devices, novel MOS device architectures (double and multiple gate, vertical, ballistic), circuit/device interaction and co-optimization, high-mobility channel engineered devices, SOI, SGOI, and SiON devices; SiGe, Ge, and strained devices. 3D integrated circuits.

Process & Integration

Front-end and back-end processes for fabrication of logic memory and 3D integrated circuits, including: substrate technologies, gate dielectrics, high k, gate stack, junction technology, cleaning and surface preparation, litography, etching, isolation technologies, thin dielectrics, shallow junctions, silicides, 3D integration, interconnects, low k dielectrics, advances in integration for ULSI; SOI, SGOI; advanced/novel memory process integration; logic and mixed-mode IC manufacturing; RF integration (passives, active devices); photonics integration; multilevel interconnects, advanced packaging.

Microwave and power solid state devices

RF CMOS, analog and mixed signal devices, passives, antennas, filters, RF MEMS, Bipolar, BiCMOS, smart power devices, high-voltage, high power devices, high temperature operation, SiC devices, CMOS compatible power devices, IC cooling. Discrete and integrated high power/current/voltage devices. Integrated RF components including inductors, capacitors,

and switches. Note: Microwave includes millimeter wave and shorter wavelength (frequencies up to the THz region).

Modelling and Simulation

Numerical, analytical and statistical modeling of solid-state electronic and optoelectronic devices, quantum mechanical and non-stationary transport phenomena, ballistic transport, compact circuit modeling for devices and interconnects, modeling and simulation of front-end and back-end fabrication processes, electro-thermal modeling and simulation.

Characterization, Reliability and Yield

Characterization techniques, parameter extraction, advanced test structures and methodologies, reliability issues for new materials and devices (reliability of high-k and low-k materials), reliability of advanced interconnects, ESD, soft errors, noise and mismatch behavior, bias temperature inestabilities, EMI, defect monitoring and control, metrology, impact of back-end processing on devices, manufacturing technologies for reliability, physics of failure analysis.

Advanced and Emerging Memories

Novel memory cell concepts, embedded and stand-alone memories, DRAM, FeRAM, MRAM, PCRAM, CBRAM, Flash, SONOS, nanocrystal memories, single and few electron memories, 3D IC stacks, organic memories, NEMS-based device, 3D integration, reliability and modeling.

MEMS, Bio-sensors and Display Technologies

Design, fabrication, modeling, reliability and packaging of all physical sensors and MEMS categories, bio-sensors for chemical, molecular and biological applications, BioMEMS, devices and technologies for lab-on-chip, integration of detectors, sensors, and actuators, CCDs and CMOS imagers, optical on chip communication, display technologies, TFTs, organic electronics, flexible substrate electronics, SoC and SiP packaging, microsystem packaging. Topics of interest in the MEMS area include resonators, switches, and passives for RF applications, integrated sensors, micro-optical devices, micro-fluidic and biomedical devices, micro power generators and energy harvesting devices, with particular emphasis on integrated implementations.

Conference Overview

Optoelectronic and photonic devices

Compound semiconductors (GaAs, InP, GaN, SiC, alloys) and optoelectronic devices, including photovoltaic devices.

Emerging non-CMOS devices and technologies

Nanotubes, nanowires and nanoparticles for electronic, optoelectronic and sensor applications, materials and device related issues, single-electron, molecular and quantum devices, nanophotonics, spintronics, self-assembling methods, photonic devices. New device characterization techniques and performance evaluation methodologies. Energy harvesting.

Carbon-based devices

The latest devices based on carbon carbon nanotubes and graphene. Digital and and analog devices, high frequency devices based on carbon nanotubes and graphene including THz and optoelectronic devices.

All meals and refreshments will be served, for all the attendees, at scheduled times during the conference program, in Foyer Grand Ballroom and Restaurants (Cucina, Champions and JW Stakehouse)

SOCIAL PROGRAM

WELCOME RECEPTION, TUESDAY, SEPT. 17TH

The Welcome Reception will take place on Tuesday evening at Athenee Palace Hilton, downtown Bucharest.

Transportation to the location will be provided. Bus departure from the conference venue (JW Marriott Bucharest Grand Hotel) will be at 19:00.

Return will be at 23:00 to conference venue (JW Marriott Bucharest Grand Hotel).

Meals and Refreshments

GALA DINNER, Wednesday, Sept. 18th

The Gala dinner will be served on Wednesday evening at Ştirbey Palace.

Transportation to the location will be provided. Bus departure from the conference venue (JW Marriott Bucharest Grand Hotel) will be at 19:00.

Return will be from 23:00 to 24:00 to conference venue (JW Marriott Bucharest Grand Hotel).

The goal of the executive round table **"Europe as Engine of Innovation in the Semiconductor Area"** is to emphasize the strength and sustainability of the semiconductor industry in Europe. The choice of the event which embeds this plenary panel is far from being neutral; ESSCIRC-ESSDERC is the major meeting point of the semiconductor scientists in Europe. The distinguished panelists are (in alphabetical order):

- Jo De Boeck, Senior Vice President and Chief Technology Officer, IMEC, Belgium
- Thierry Collette, Vice President, LETI, France
- Philippe Magarshack, Executive Vice President, STMicroelectronics, France
- Lothar Pfitzner, Head of Semiconductor Manufacturing, Fraunhofer, Germany
- Reinhard Ploss, Chief Executive Officer, Infineon Technologies, Germany
- Hans Rijns, Chief Technology Officer, NXP Semiconductors, The Netherlands
- Andreas Wild, Executive Director, ENIAC Joint Undertaking, Belgium

The round table will be moderated by Andreia Cathelin, Senior Member of the Technical Staff, STMicroelectronics Crolles, and Jihad Haidar, Vice President and Managing Director, Infineon Technologies Romania.

Automotive electronics and energy efficiency

Dr. Reinhard Ploss, CEO Infineon

1. Semiconductors at the service of higher safety, more comfort, and low emission mobility (e.g. increased semiconductors in car for energy efficiency in engine, safety and body);

2. Semiconductors at the service of reduced emissions and a more efficient energy usage in the modern society (e.g. semiconductors in energy supply chain for higher efficiency);

3. What technologies are in place for different power/frequency/temperature etc… levels (e.g. Power Technologies roadmap, new materials etc.);

4. Innovation on technology (FE and BE) required to tackle the future challenges/bottleneck (our Power300 with thin wafer, new packages, system oriented thinking, etc.);

5. Examples with applications in automotive (Electric car) or Energy Grid showing the end user benefits (this can refer to components and/or technologies from Infineon).

Dr. Reinhard Ploss joined Siemens/Infineon in 1986, working in Munich as a process engineer with focus on chip manufacturing.

In 1992 he moved on to Villach, Austria, where he started in chip manufacturing and took over the position as Head of Technology in 1993. He returned to Munich in 1996 and took charge of the Power Semiconductor Business Unit, focusing on development and manufacturing. In 1999, Dr. Reinhard Ploss was appointed Head of the Industrial Power Business Unit as well as President of eupec GmbH Co. KG, a subsidiary of Infineon.

In 2000, Dr. Reinhard Ploss took over as President of the Automotive & Industrial Business Group of Infineon. From 2005 on, he held responsibility for manufacturing, development and operational management in the Automotive, Industrial & Multimarket Business Group.

In June 2007, Dr. Reinhard Ploss was appointed to the Management Board of Infineon, with responsibilities for manufacturing activities. In addition, he became Labor Director and Head of Research & Development. He remains responsible for these three areas to the present day.

Since October 1, 2012, Dr. Reinhard Ploss is Chief Executive Officer of Infineon Technologies AG.

FinFETs: Technology and Circuit Design Challenges

Witek Maszara, GLOBALFOUNDRIES

It took quarter of a century for multi-gate transistor to make it from first demonstration in research to a product – 22nm technology node microprocessor in 2012. FinFETs offer superior performance over incumbent planar devices due to their significantly improved electrostatics. FinFET technology faced two key barriers to their implementation in products: demanding process integration and its significant impact on layout and circuit design methodology. In this paper we focus on challenges and tradeoffs in both of these areas. Fin shape, pitch, isolation, doping, crystallographic orientation and stressing as well as device parasitics, performance and patterning approaches will be discussed. Implementation of high mobility materials for finFET devices will also be briefly reviewed as well as design challenges for logic and SRAM circuits.

Witold (Witek) P. Maszara has received MS degree in Electronics from Technical University of Wroclaw, Poland, and PhD degree from University of Kentucky in EE. Co-author of 100+ papers, author of over 50 invited talks and seminars, and over 60 patents in the field of microelectronics. Served as Technical Program Chair and General Chair of IEEE International SOI Conference, Chair of IEEE IEDM's Subcommittee for Integrated Circuits and Manufacturing . Currently serving on technical committees for IEDM and VLSI Symposium on Technology. Member of advisory boards for Semiconductor Research Corporation, Sematech, National Science Foundation, IMEC (Belgium) and INMP (Stanford U.) for broad range of semiconductor technology programs. Current areas of interest: CMOS logic technology, dense embedded memory and integrated photonics for deep submicron CMOS applications. He is presently employed at GLOBALFOUNDRIES as Principal Member of Technical Staff. Currently manages GLOBALFOUNDRIES Exploratory Research for 7nm technology node and beyond, covering Device, Interconnect, Memory and Photonics research.

Carbon Electronics - what can we do with it?

Wilfried Haensch, IBM

The slowdown of scaling intensified the search for the “next switch”. The dream is, of course, to find a new switching element that can replace the conventional transistor. Preferably without any change of the existing infra-structure – new materials and fabrication methods would be tolerated. Due to its superb thermal and electrical transport properties carbon in form of graphene or carbon nanotubes (CNTs) is considered as a natural successor of the current available technology solutions in the digital and RF space. In both, graphene and CNTs, devices can be build that resemble very closely the existing device structures and would therefore fit into the existing technology ecosystem without major interruptions. However, graphene and CNT based device technologies come with their own challenges that have to be overcome to insert them into a technology. I will discuss current progress in graphene and CNT device research and will provide insight in possible application spaces for these materials. A brief outlook is given on how graphene could be used for none conventional device architecture solutions.

Wilfried Haensch received his Ph.D. in 1981 from the Technical University of Berlin, Germany in the field of theoretical solid state physics. He started his career in Si technology 1984 at SIEMENS corporate research Munich. There he worked on high field transport in MOSFETs. In 1990 he joined the DRAM alliance between IBM and SIEMENS to develop quarter micron 64M DRAM. From there he moved in 1996 to INFINEON’s manufacturing facility in Richmond VA to be involved in the production of various generations of DRAM. In 2001 he joint IBM TJ Watson Research Center to lead a group for novel devices and applications. In this function he was responsible for the exploration of device concepts for 15nm node and beyond, new scaling concepts for memory and logic circuits, including 3D integration. He is currently responsible for post CMOS device solution and Si technology extensions. This includes carbon electronics for RF and digital applications and optical and electrical material properties of graphene and carbon nano tubes. He is the author of a text book on transport physics and author/co-author of more than 100 publications. He was awarded the Otto Hahn Medal for outstanding Research in 1983. He was named IEEE Fellow in 2012.

Nanometer-scale InGaAs Field-Effect Transistors for THz and CMOS technologies

Jesus A. del Alamo, MIT, USA

Integrated circuits based on InGaAs Field Effect Transistors are now widely used in the RF front-ends of smart phones and other mobile platforms, wireless LANs, high data rate fiber optic links and many defense and satellite communication systems. InGaAs ICs are also under intense research for new millimeter-wave applications such as collision avoidance radar and gigabit WLANs. In the last few years, as Si CMOS faces mounting difficulties to maintain its historical scaling path, InGaAs-channel MOSFETs have emerged as a credible alternative for mainstream logic technology capable of scaling to the 10 nm node and below. To get to this point, fundamental technical problems had to be solved though there are still many challenges that need to be addressed before the first non-Si CMOS technology becomes a reality. The intense research that this exciting prospect is generating will also reinvigorate the long march of InGaAs FETs towards the first true THz electronics technology. This talk will review progress and challenges of InGaAs-based FET technology for THz and CMOS.

Jesus A. del Alamo obtained a Telecommunications Engineer degree from the Polytechnic University of Madrid in 1980 and MS and PhD degrees in Electrical Engineering from Stanford University in 1983 and 1985, respectively. From 1985 to 1988 he was with NTT LSI Laboratories in Atsugi (Japan) and since 1988 he has been with the Department of Electrical Engineering and Computer Science of Massachusetts Institute of Technology where he is currently Donner Professor and MacVicar Faculty Fellow. His current research interests are centered on nanoelectronics based on compound semiconductors. He is also investigating the potential of online laboratories for science and engineering education.Prof. del Alamo was an NSF Presidential Young Investigator. He is a member of the Royal Spanish Academy of Engineering and Fellow of the IEEE. He currently serves as Editor of IEEE Electron Device Letters.

Joint Plenary Talks

MEMS for automotive and consumer electronics

Stefan Finkbeiner, Bosch

MEMS, tiny micro-electro-mechanical systems that function as miniature machines, are showing up in all facets of our daily lives — Established in Automotive applications since almost 30 years, they can be found today predominantly in smartphones, tablets, cameras, laptops, video games! Your favorite consumer product likely contains more than a half-dozen MEMS. From accelerometers and gyroscopes that 'interpret' motion into the digital realm, to magnetic compasses, pressure sensors and MEMS microphones, MEMS sensors have dramatically improved the user experience with electronic devices.

Some of the addressed aspects:

- Current MEMS sensor context in smartphones & automotive.
- Evolution of use cases – introduction of new sensor types and addressing of new applications.
- The concept of Application Specific Sensor Nodes (ASSN's).
- How will the IoT emerging market impact or will be impacted by sensor node developments.

CEO and General Manager of Bosch Sensortec GmbH, **Dr. Stefan Finkbeiner** was born in 1966 in Freudenstadt, Germany. He received his Diploma in Physics from the University of Karlsruhe in 1992. He then studied at the Max-Planck-Institute in Stuttgart and received his PhD in Physics from the University of Stuttgart in 1995.

Dr. Finkbeiner joined Robert Bosch GmbH in 1995 and has been working for more than 17 years in different positions related to the research, development, manufacturing, and marketing of sensors. Senior positions at Bosch have included Director of Marketing for sensors, Director of Corporate Research in microsystems technology, and Vice President of Engineering for sensors.

Before joining Bosch Sensortec GmbH end of 2012 as CEO and General Manager he was the CEO of Akustica, a Bosch Group company which develops MEMS microphones for consumer electronics applications and is located in Pittsburgh, PA, USA.

Cyborg insects and other things: building interfaces between the synthetic and the multicellular

M. Maharbiz, University of California Berkeley

Michel M. Maharbiz is an Associate Professor with the Department of Electrical Engineering and Computer Science at the University of California, Berkeley.

He received his Ph.D. from the University of California at Berkeley for his work on microbioreactor systems under Professor Roger T. Howe (EECS) and Professor Jay D. Keasling (ChemE). His work led to the foundation of Microreactor Technologies, Inc. which was acquired in 2009 by Pall Corporation. From 2003 to 2007, Michel Maharbiz was an Assistant Professor at the University of Michigan, Ann Arbor. He is the co-founder of Tweedle Technologies, Cortera Neurotech and served as vice-president for product development at Quswami, Inc. from July 2010 to June 2011.

Prof. Maharbiz is a Bakar Fellow and was the recipient of a 2009 NSF Career Award for research into developing microfabricated interfaces for synthetic biology. His group is also known for developing the world's first remotely radio-controlled cyborg beetles. This was named one of the top ten emerging technologies of 2009 by MIT's Technology Review (TR10) and was in Time Magazeine's Top 50 Inventions of 2009. Dr. Maharbiz has been a GE Scholar and an Intel IMAP Fellow. Professor Maharbiz's current research interests include building micro/nano interfaces to cells and organisms and exploring bio-derived fabrication methods. Michel's long term goal is understanding developmental mechanisms as a way to engineer and fabricate machines.

ESSDERC Plenary Talks

Ultrahigh-Voltage SiC Devices for Future Power Infrastructure

Tsunenobu Kimoto, Kyoto University, Japan

High-efficiency electric power conversion is an essential technology for energy saving. The efficiency of power converters/inverters strongly relies on the performance of power semiconductor devices employed in the power electronic systems. Silicon carbide (SiC) is a newly-emerging wide bandgap semiconductor, by which high-voltage, low-loss power devices can be realized owing to its superior properties. It is expected that SiC unipolar devices will replace Si unipolar/bipolar devices in the blocking-voltage range from 300 V to about 4500 V. For ultrahigh-voltage applications above 4500 V, SiC bipolar devices will be attractive. In this talk, recent progress in ultrahigh-voltage SiC power devices is reviewed. In particular, challenges for ultrahigh-voltage (> 20 kV) PiN diodes and power transistors are presented.

Tsunenobu Kimoto received the B.E. and M.E. degrees in Electrical Engineering from Kyoto University, Japan, in 1986 and 1988, respectively. He joined Sumitomo Electric Industries, LTD in 1988. In 1990, he started his academic career as a Research Associate at Kyoto University, and received the Ph.D. degree from Kyoto University in 1996, based on his work on silicon carbide (SiC). From 1996 to 1997, he was a visiting scientist at Linköping University, Sweden, and he is currently a Professor at Department of Electronic Science and Engineering, Kyoto University. Since 2009, he is also a core researcher of the Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program) on SiC. His main research activity includes SiC, GaN-based power devices, nano-scale Si devices, and materials for ReRAM.

Emerging Memories

Livio Baldi, Micron Semiconductor, Italy

Solid state memories are a critical element of any computing and control system, and are becoming the prevailing tool for information storage. The variety of functions covered by memory devices has given rise to different memory typologies, all based on the principle of charge storage. However, after almost 50 years of continuous evolution, all these types of memories seem to have reached their technological limits, and a drastic change of approach is required. Emerging memories are based on different storage mechanisms, and no

clear winner has emerged yet, even if some broad trends can be identified. The main families of memories will be discussed with reference to their performance trade-offs and scalability. At the moment the large variety of alternatives is preventing the focusing of investments needed to reach the same maturity as consolidate memory types, but niche applications can be indentified that could push the technological development. Even if none of the proposed approaches seem yet really capable to fulfill the role of "unified memory", a possible future scenario will see combinations of different technologies to built specialized memory systems.

Ing. Livio Baldi graduated in Electronic Engineering in 1973 at the University of Pavia. In 1974 he joined SGS-ATES (now STMicroelectronics), in the Central R&D of Agrate Brianza. He has been responsible for the development of CMOS processes for EEPROM memories and multifunction logic. In 1999 he moved to lead the NVM Design Platform Development Group. In 2001he was put in charge of coordinating the participation of ST Italy in cooperation research projects, representing it in the MEDEA+ Steering Group- Technology and in the Support Group of the European Technology Platform (ENIAC). He has acted as consultant for the Commission in the definition of Framework Programmes and he is member of the Expert Advisory Group for Theme 4 (Nanoscience, Materials and Production Technology) of FP7. From March 31st, 2008 he has moved to Numonyx, the new ST-Intel joint venture on Flash memories, in charge of External Relations and Funding in Central R&D, and representing it in AENEAS and CATRENE. From 2010, following the acquisition of Nymonyx by Micron Technology, he fills the same position in Micron Semiconductor Italia. He holds 33 US patents, 17 European patents, and is author of more than 70 papers and communications to conferences.

2D Electronics: graphene and beyond

Kaustav Banerjee, University of California, Santa Barbara

Graphene – composed of a single layer of carbon atoms arranged in a hexagonal pattern, is the basic material for the family of low-dimensional allotropes of carbon known as carbon nanomaterials. These graphene based nanomaterials have extraordinary physical properties that can be exploited for their exciting prospects for a variety of applications. This

talk will highlight and discuss the unique prospects of graphene based nanomaterials for designing next generation low-power, low-loss and ultra energy-efficient active and passive devices targeted for designing next-generation "green electronics". The discovery of Graphene has also opened up a new era for a wide range of 2D nanomaterials and their unprecedented electronic applications. This talk will also provide a brief overview of such materials and related opportunities, especially in the electronics domain.

Kaustav Banerjee is Professor of Electrical and Computer Engineering and Director of the Nanoelectronics Research Lab at the University of California, Santa Barbara (UCSB). Initially trained as a physicist, he received the Ph.D. degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley, in 1999. Prior to joining the UCSB Faculty in 2002, he was a Research Associate at the Center for Integrated Systems in Stanford University during 1999-2001. His research interests include nanometer-scale issues in CMOS VLSI as well as emerging nanoelectronics. Prof. Banerjee's ideas and innovations chronicled in over 250 publications have not only received thousands of citations but also have played a decisive role in steering worldwide research. He was elected a Fellow of IEEE in Fall 2011, and has served as a Distinguished Lecturer of the IEEE Electron Devices Society since 2008. Prof. Banerjee is one of five engineers worldwide to receive the Friedrich Wilhelm Bessel Research Award from Alexander von Humboldt Foundation, Germany, in 2011 for his outstanding contributions in nanoelectronics. More information about him and his research can be found at: http://nrl.ece.ucsb.edu/

Monday, Sept. 16, 2013

All tutorials are "Full-Day"

MEMS and Sensors: technology and applications

09:30 - 10:50	"Resonant piezoelectric MEMS" - Prof. Gianluca Piazza, Carnegie Melon, USA
10:50 - 11:10	Coffee break
11:10 - 12:30	"MEMS Oscillators, Mixers and Filters" - Dr. Ashwin Seshia, University of Cambridge, UK
12:30 - 14:00	Lunch
14:00 - 14:40	"Resonant transistors for low power radios and sensing" - Prof. Adrian Ionescu, EPF Lausanne, Switzerland & Dr. Joost Van Beek, NXP, The Netherlands
14:40 - 15:40	"Microwave MEMS and applications" - Prof. Dan Neculoiu, IMT & University Politehnica Bucharest, Romania
15:40 - 16:00	Coffee break
16:00 - 17:00	"MEMS and Sensors - emerging technologies and applications" - Prof. Julian Gardner, Warwick University, UK

High Voltage technologies

09:30 - 10:50	"Status and perspective of silicon-based high voltage devices for highest efficiency applications" - Dr. Gerald Deboy, Infineon, Austria
10:50 - 11:10	Coffee break
11:10 - 12:30	"Diamond Power Devices" - Dr. Mihai Brezeanu, Honeywell, Romania
12:30 - 14:00	Lunch
14:00 - 15:20	"High Voltage GaN HEMT devices and modelling" - Dr. Stephen Sque, NXP, Netherland
15:40 - 16:00	Coffee break
15:40 - 17:00	"SiC Ultra High Voltage devices and applications" - Prof. Phil Mawby, University of Warwick, UK

Graphene

09:30 - 10:50	"Graphene technology: challenges & opportunities" - Dr. Stephan Hofmann, University of Cambridge
10:50 - 11:10	Coffee break

ESSDERC Tutorials

11:10 - 12:30	“Graphene Electronic Devices I” - Prof. Max Lemme, Universität Siegen, Germany
12:30 - 14:00	Lunch
14:00 - 15:20	“Graphene Electronic Devices II” - Prof. Max Lemme, Universität Siegen, Germany
15:40 - 16:00	Coffee break
15:40 - 17:00	“Graphene passive devices for Teraherz applications” - Prof. Julien Perruisseau-Carrier, EPFL, Switzerland

Friday, Sept. 20, 2013

Potential of Eastern European Countries in Key Enabling Technologies

Organizer:

Ion Bogdan, *TU Iasi, Romania*

Full day Workshop (9:00 – 18:00)

The aim of the workshop is to offer scientists form East European countries an opportunity to meet and to present, on the occasion of ESSCIRC/ESSDERC, the main directions of research in the domain of microelectronics in their regions/countries. A special presentation will be made by Dr. Andreas Wild, executive manager of ENIAC JU. The speakers come from most of the East European countries and represent reputed research institutions and universities. The presentations and the discussions that will follow will reveal state-of-the-art of the research in East European countries and are intended to open new ways for a stronger cooperation between scientists working in the semiconductor domain.

Speakers at the workshop:

- Andreas Wild, Executive Director of the ENIAC Joint Undertaking
- Anelia Pergoot, ZMD Eastern Europe, Bulgaria
- Ion Tighineanu, Academy of Science, Moldova Republic
- Piotr Grabiec: Instytut Technologii Elektronowej (ITE), Warsaw
- Raluca Müller, National Institute for R&D in Microtechnologies (IMT Bucharest), Romania
- Aleksandr Korotkov, Sankt Petersburg State Polytechnical University, Russia
- Valentin Turin, TCAD- Educational and Research Lab. in Micro- and Nanoelectronics State University ESPC, Orel, Russia
- Volkan Ozguz, Nanotechnology Research and Application Center, Sabanci University, Turkey
- Istvan Barsony, Institute of Technical Physics and Materials Science, MFA, Budapest, Hungary

- Peeter Ellervee, Tallin University of Technology, Estonia
- Daniel Donoval, Slovak University of Technology, Bratislava, Slovakia
- Ashkhen Yesayan, Institute of Radiophysics and Electronics, NAS, Armenia

MOS-AK Compact Modeling Workshop

Organizers:

Wladek Grabinski, *MOS-AK Group*, **and Prof. Andrei Vladimirescu,** *R&D Scientific Coordinator*
Full day Workshop (9:00 – 18:00)

Par4CR Workshop on Cognitive Radio

Organizer:

Peter Baltus, *TU Eindhoven, The Netherlands*

Full day Workshop (9:00 – 18:00)

By the year 2020, mobile and wireless communications will play a central role in all aspects of European citizen's lives. Realization of this vision demands a major shift from the current concept of "anywhere - anytime" to a new paradigm of "any network - any device", with relevant content and context in a secure and trustworthy manner.

As more devices "go wireless" and human wireless networks proliferate at unprecedented speed more bandwidth and better use of the RF spectrum will be required to avoid future "wireless traffic jams". In this context the realization of cognitive radio (CR) is essential to meet the requirements of future wireless communication infrastructures. Software defined radio (SDR) should be a step on the path towards CR. For these reasons the European Universities and Industrial Companies organized a partnership in order to develop software defined radio architecture toward cognitive radio (Par4CR). This project is funded by EU and organized in the frame of Industry-Academia Partnerships and Pathways (IAPP). Par4CR brings together a consortium of seven major European players to perform a joint research programme and exchange knowledge on technologies crucial for the development of software defined radio and cognitive radio. The seven partners are from industry: NXP Semiconductors, France; IMST GmbH, Germa-

ny; Catena Holding, the Netherlands and Sweden, and from academia: Eindhoven University of Technology, the Netherlands; ESIEE, France; TNO, the Netherlands and Institute of Electron Technology, ITE, Poland.

In the workshop final results from the Par4CR project will be presented together with views on the subject from leaders in this field. The workshop will present the last scientific results from the Par4CR project on different subjects related to the Cognitive Transceivers Technologies, including signal conversion, digital signal processing technologies, RF front-end and antenna design.

FP7 Variability and Reliability Showcase

Organizer:

Asen Asenov, *U Glasgow, UK*, **and Antonio Rubio,** *UPC Barcelona, Spain*

Full day Workshop (9:00 – 18:00)

i-RISC Workshop on Innovative Reliable Chip Designs from Unreliable Components

Organizers:

Valentin Savin, *CEA LETI, Grenoble, France,* **and Sorin Cotofana,** *TU Delft, The Netherlands*

Full day Workshop (9:00 – 18:00)

The ongoing miniaturization of data processing and storage devices and the imperative of low-energy consumption can only be sustained through low-powered components. However, lower supply voltages combined with variations in technological process of emerging nanoelectronic devices make them inherently unreliable. As a consequence, the nanoscale integration of chips built out of unreliable components has emerged as one of the most critical challenges for the next-generation electronic circuit design. To make such nanoscale integration economically viable, new solutions for efficient and fault-tolerant data processing and storage must be investigated.. Workshop Purpose: The i-RISC Workshop addresses the problem of reliable computing with unreliable components, which is a crucial issue for the long-term development of computing technology. The Workshop main goal is to explore the synergistic utilization of information and coding theory and techniques, traditionally utilized to improve the

reliability of communication systems, and circuit and system theory and design techniques in order to create reliable/predictable hardware. The aim is to enable the development of innovative fault-tolerant solutions at both circuit- and system-level that are fundamentally rooted in mathematical models, algorithms, and techniques of information and coding theory.

In the Quest for Zero Power: Enabling Smart Autonomous System Applications

Organizer:

Adrian Ionescu, *EPFL, Switzerland*

Full day Workshop (9:00 – 18:00)

Keynote

- The role of new materials in nanoelectronics – Robert Westervelt, Harvard University

Session 1: Smart Autonomous Systems

- Technology challenges for a smarter planet – Walter Riess, IBM Zürich
- Roadmaps for future nanolectronics – Denis Rousset, Catrene, Paris

Session 2: Ultra low power computation & communication

- Computing with NEMS –Hervé Fanet, CEA-LETI, Grenoble
- Graphene: an enabler of low power devices? Max Lemme, University of Siegen
- Tunnel FET versus MOSFET: a critical review – Giorgio Baccarani, University of Bologna

Session 3: Heterogenous integration

- The e-BRAINS project - Peter Ramm, Fraunhofer Research Institution for Modular Solid State Technologies EMFT, Munich
- Heterogeneous integration for infrared sensors, Adriana Lapadatu, SINTEF

Session 4: Low power sensors and energy scavenging for system integration

- Energy harvesting for self-powered sensor systems–

Rob van Schaijk, IMEC-NL

- Carbon-based sensors, Cosmin Roman, ETH Zürich
- Chemical sensors: towards the 6th sense system – Max Fleischer, Siemens
- Mechanical energy harvesiting– Eric Yeatman, Imperial College

Session 5: New opportunities in Horizon 202o for Smart Systems

- Priorities and funding strategies in Horizon 2020 for Smart Systems - Dirk Beernaert, European Commission - tbc

SINANO Workshop: "Nanowires for Logic, Memory and New Functionalities"

Organizer:
Francis Balestra, *Sinano Institute - Grenoble INP/ CNRS*

Full day Workshop (9:00 – 18:00)

This Workshop is supported by the European Institute of Nanoelectronics SINANO (www.sinano.eu) and aims at discussing state-of-the art results and disruptive achievements in the field of Nanowires for very low power and high performance logic and memory, and for adding new functionalities to CMOS in the More than Moore domain (sensing, energy harvesting, RF and e-cooling).

8:50	"Introduction", Francis Balestra, Sinano Institute
9:00	"Nanowire devices for the 10nm technology node and beyond", Sylvain Barraud, CEA-LETI -9:30 "Extending Moore's law: Nanowires to the rescue", Nadine Collaert, IMEC
10:00	"Energy efficient electronics: prospects and challenges of superlattice nanowire FETs", Elena Gnani, Giorgio Baccarani, IUNET-University of Bologna
10:30	Coffee break
11:00	"Complementary Strained Si nanowire TFETs and Inverters", Qing-Tai Zhao, Siegfried Mantl, Forschungszentrum Juelich

11:30	“Challenges and opportunities in InAs Tunnel FETs: a simulation study”, Marco Pala, IMEP-LAHC, Grenoble INP/CNRS, David Esseni, IUNET-University of Udine
12:00-13:30	Buffet lunch
13:30	“Nanowires for sensing applications”, Per-Erik Hellström, Mikael Ostling, KTH
14:00	“Piezoelectric nanowires for mechanical energy harvesting “, Gustavo Ardila, IMEP-LAHC, Grenoble INP-Minatec
14:30	“Nanowires and nanostructured Si for RF applications”, Androula Nassiopoulou, IMEL/NCSR Demokritos
15:00	“e-cooling and impact of low dimensionality”, Evan Parker, David Leadley, University of Warwick
15:30	**End of Workshop**

Tuesday, September 17

Wednesday, September 18

Thursday, September 19

ESSDERC Technical Program

Tuesday, September 17

Emerging FET Devices

Session Code: A3L-A

Location: Room A

Date & Time: Tuesday, September 17
13:00 - 14:00

Chair(s): Radu Sporea
University of Surrey
Andreas Schenk
ETHZ

13:00 **Performance Limit of Parallel Electric Field Tunnel FET and Improvement by Modified Gate and Channel Configurations**
Yukinori Morita, Takahiro Mori, Shinji Migita, Wataru Mizubayashi, Akihito Tanabe, Koichi Fukuda, Takashi Matsukawa, Kazuhiko Endo, Shin-Ichi O'Uchi, Yongxun Liu, Meishoku Masahara, Hiroyuki Ota
National Institute of Advanced Industrial Science and Technology, Japan

13:20 **On the Optimization of SiGe and III-V Compound Hetero-Junction Tunnel FET Devices**
Alberto Revelant[2], Pierpaolo Palestri[2], Patrik Osgnach[1], Daniel Lizzit[2], Luca Selmi[2]
[1]DIEGM, Università degli Studi di Udine, Italy; [2]Università degli Studi di Udine, Italy

13:40 **Characterization of Border Traps in III-V MOSFETs Using an RF Transconductance Method**
Sofia Johansson, Jiongjiong Mo, Erik Lind
Lund University, Sweden

Tuesday, September 17

GaN and NEMS

Session Code: A3L-C

Location: Room C

Date & Time: Tuesday, September 17
13:00 - 14:00

Chair(s): Gunnar Malm
KTH Royal Institute of Technology
Henryk Przewlocki
Institute of Electron Technology

13:00 **Electron Delay Analysis and Image Charge Effect in AlGaN/GaN HEMT on Silicon Substrate**
Alain Agboton[1], Nicolas Defrance[1], Phillipe Altuntas[1], Vannessa Avramovic[1], Adrien Cutivet[1], Rezky Ouhachi[1], Jean-Claude De Jaeger[1], Samira Bouzid-Driad[2], Hassan Maher[2], Michel Renvoise[2], Peter Frijlink[2]
[1]Intitut d'Electronique,de Microélectronique et de Nanotechnologie, France; [2]OMMIC, France

13:20 **Influence of Fluorine-Based Dry Etching on Electrical Parameters of AlGaN/GaN-on-Si High Electron Mobility Transistors**
Davide Bisi[2], Matteo Meneghini[2], Antonio Stocco[2], Giulia Cibin[2], Alessio Pantellini[1], Antonio Nanni[1], Claudio Lanzieri[1], Enrico Zanoni[2], Gaudenzio Meneghesso[2]
[1]Selex E.S., Italy; [2]Università degli Studi di Padova, Italy

13:40 **Impact of Process Variability on a Frequency-Addressed NEMS Array Sensor Used for Gravimetric Detection**
Olivier Martin[2], Eric Colinet[1], Eric Sage[2], Cécilia Dupré[2], Patrick Villard[2], Sébastien Hentz[2], Laurent Duraffourg[2], Thomas Ernst[2]
[1]Apix Technology, France; [2]CEA-LETI, France

Tuesday, September 17

Emerging FET-like Modeling

Session Code: A3L-F

Location: Room TM

Date & Time: Tuesday, September 17
13:00 - 14:20

Chair(s): Bernd Meinerzhagen
Technical Unversity of Braunschweig
Wladek Grabinski
Nanolab, EPFL

13:00 **Complementary N- and P-Type TFETs on the Same InAs/Al0:05Ga0:95Sb Platform**
Emanuele Baravelli, Elena Gnani, Roberto Grassi, Antonio Gnudi, Susanna Reggiani, Giorgio Baccarani
Università di Bologna, Italy

13:20 **Boosting InAs TFET on-Current Above 1 mA/μm with No Leakage Penalty**
Giovanni Betti Beneventi, Elena Gnani, Antonio Gnudi, Susanna Reggiani, Giorgio Baccarani
Università di Bologna, Italy

13:40 **Full-Band Simulation of P-Type Ultra-Scaled Silicon Nanowire Transistors**
Áron Szabó, Mathieu Luisier
ETH Zürich, Switzerland

14:00 **Gate Stack Optimization to Minimize Power Consumption in Super-Lattice FETs**
Pasquale Maiorano, Elena Gnani, Antonio Gnudi, Susanna Reggiani, Giorgio Baccarani
Università di Bologna, Italy

Tuesday, September 17

ESSDERC Keynote: T. Kimoto (Kyoto Univ.)

Session Code: A4L-E

Location: Room CT

Date & Time: Tuesday, September 17
14:20 - 15:20

Chair(s): Florin Udrea
University of Cambridge

14:20 **Ultrahigh-Voltage SiC Devices for Future Power Infrastructure**
Tsunenobu Kimoto
Kyoto University, Japan

Tuesday, September 17

ESSDERC Invited Session I

Session Code: A5L-E

Location: Room CT

Date & Time: Tuesday, September 17
15:50 - 16:50

Chair(s): Gunnar Malm
KTH Royal Institute of Technology

15:50 **Investigation of Carbon-Silicon Schottky Diodes and Their Use as Chemical Sensors**
Georg S. Duesberg, Hye-Young Kim, Kangho Lee, Niall McEvoy, Sinéad Winters, Chanyoung Yim
Trinity College Dublin, Ireland

16:20 **Modeling and Characterization of Hot-Carrier Stress Degradation in Power MOSFETs**
Susanna Reggiani[2], Elena Gnani[2], Antonio Gnudi[2], Giorgio Baccarani[2], Stefano Poli[1], Rick Wise[1], Ming-Yeh Chuang[1], Weidong Tian[1], Marie Denison[1]
[1]Texas Instruments, United States; [2]Università di Bologna, Italy

Tuesday, September 17

Technologies and Devices for RF and Power Applications

Session Code: A6L-E

Location: Room CT

Date & Time: Tuesday, September 17
16:50 - 18:50

Chair(s): Gaudenzio Meneghesso
University of Padova
Gianmauro Pozzovivo
Infineon Technologies Austria

16:50 **An Experimental Study of Integrated DMOS Transistors with Increased Energy Capability**
Timo Zawischka[1], Martin Pfost[1], Michael Ebli[1], Dragos Costachescu[2]
[1]Hochschule Reutlingen, Germany; [2]Robert Bosch GmbH, Germany

17:10 **Porous Si Dielectric Parameter Extraction for Use in RF Passive Device Integration: Measurements and Simulations**
Panagiotis Sarafis, Emmanouel Hourdakis, Androula Nassiopoulou
National Center for Scientific Research, Demokritos - IMEL, Greece

17:30 **4H-SiC MESFET Specially Designed and Fabricated for High Temperature Integrated Circuits**
Mihaela Alexandru, Viorel Banu, Philippe Godignon, Miquel Vellvehi, Jose Millan
CNM-IMB CSIC, Spain

17:50 **Advantage of TiN Schottky Gate Over Conventional Ni for Improved Electrical Characteristics in AlGaN/GaN HEMT**
Takamasa Kawanago, Kuniyuki Kakushima, Yoshinori Kataoka, Akira Nishiyama, Nobuyuki Sugii, Hitoshi Wakabayashi, Kazuo Tsutsui, Kenji Natori, Hiroshi Iwai
Tokyo Institute of Technology, Japan

18:10 **Monolithic Fabrication of a Planar Gunn Diode and a pHEMT Side-by-Side**
Vasileios Papageorgiou, Ata Khalid, Matthew Steer, Chong Li, David R. S. Cumming
University of Glasgow, United Kingdom

18:30 **Impact of T-Gate Stem Height on Parasitic Gate Delay Time in InGaAs-HEMTs**
Tomohiro Yoshida, Kengo Kobayashi, Taiichi Otsuji, Tetsuya Suemitsu
Tohoku University, Japan

Tuesday, September 17

Optoelectronic and Photonic devices

Session Code: A6L-F

Location: Room TM

Date & Time: Tuesday, September 17
16:50 - 18:50

Chair(s): Ion Tiginyanu
Academy of Sciences of Moldova

16:50 **Role of Junction Depth in Light Emission from Silicon P-I-N LEDs**
Giulia Piccolo[2], Amir Sammak[1], Ray Hueting[2], Jurriaan Schmitz[2], Lis Nanver[1]
[1]Technische Universiteit Delft, Netherlands; [2]University of Twente, Netherlands

17:10 **Filter-Less Color Sensor in Standard CMOS Technology**
Graciele Batistell, Johannes Sturm
Carinthia University of Applied Sciences, Austria

17:30 **New Color Sensor Concept Based on Single Spectral Tunable Photodiode**
Andre Wachowiak, Stefan Slesazeck, Paul Jordan, Juergen Holz, Thomas Mikolajick
Namlab gGmbH & Technische Universität Dresden, Germany

17:50 **Towards Rectennas for Solar Energy Harvesting**
Naser Sedghi, Jingwei Zhang, Jason Ralph, Yi Huang, Ivona Mitrovic, Steve Hall
University of Liverpool, United Kingdom

18:10 **Photodiodes in Deep Submicron CMOS Process for Fully Integrated Optical Receivers**
Waqas Ahmad, Markus Törmänen, Henrik Sjöland
Lund University, Sweden

ESSDERC Technical Program

Wednesday, September 18

ESSDERC Keynote: L. Baldi (Micron)

Session Code: B3L-E

Location: Room CT

Date & Time: Wednesday, September 18
10:50 - 12:30

Chair(s): Raluca Muller
IMT Bucharest

10:50 **Emerging Memories**
Livio Baldi[1], Gurtej Sandhu[2]
[1]Micron Semiconductor Italia, Italy; [2]Micron Technology inc., United States

Wednesday, September 18

Emerging Devices

Session Code: B4L-A
Location: Room A
Date & Time: Wednesday, September 18
14:00 - 15:00
Chair(s): Francois Andrieu
CEA-LETI
Nadine Collaert
IMEC

14:00 **Physical Understanding of Electron Mobility in Uniaxially Strained InGaAs-OI MOSFETs**
Sanghyeon Kim[2], Masafumi Yokoyama[2], Yuki Ikku[2], Ryosho Nakane[2], Osamu Ichikawa[1], Takenori Osada[1], Masahiko Hata[1], Mitsuru Takenaka[2], Shinichi Takagi[2]
[1]Sumitomo Chemical Co. Ltd., Japan; [2]University of Tokyo, Japan

14:20 **Scalability of Ultra-Thin-Body and BOX InGaAs MOSFETs on Silicon**
Lukas Czornomaz[1], Nicolas Daix[1], Pranita Kerber[2], Kevin Lister[1], Daniele Caimi[1], Christophe Rossel[1], Marilyn Sousa[1], Emanuele Uccelli[1], Jean Fompeyrine[1]
[1]IBM Research GmbH, Switzerland; [2]IBM T.J. Watson Research Center, United States

14:40 **The Coupled Atom Transistor: a First Realization with Shallow Donors Implanted in a FDSOI Silicon Nanowire**
Benoit Voisin[2], Benoit Roche[2], Eva Dupont-Ferrier[2], Benoit Sklénard[4], Manuel Cobian[1], Xavier Jehl[2], Olga Cueto[3], Romain Wacquez[3], Maud Vinet[3], Yann-Michel Niquet[1], Silvano De Franceschi[2], Marc Sanquer[2]
[1]CEA-INAC-SP2M, France; [2]CEA-INAC-SPSMS, France; [3]CEA-LETI, France; [4]STMicroelectronics, France

Wednesday, September 18

Processing & Integration

Session Code: B4L-B

Location: Room B

Date & Time: Wednesday, September 18
14:00 - 15:00

Chair(s): Per-Erik Hellström
KTH Royal Institute of Technology
Simon Deleonibus
CEA

14:00 **Novel Low Temperature 3D Wafer Stacking Technology for High Density Device Integration**
Ionut Radu[3], Gweltaz Gaudin[3], William Van Den Daele[3], Fabrice Letertre[3], Carlos Mazure[3], Lea Di Cioccio[1], Thomas Lacave[1], Frederic Mazen[1], Pascal Scheiblin[1], Thomas Signamarcheix[1], Sorin Cristoloveanu[2]
[1]CEA-LETI, France; [2]IMEP-LAHC, France; [3]SOITEC, France

14:20 **Mobility Enhancement by Integration of TmSiO IL in 0.65nm EOT High-k/Metal Gate MOSFETs**
Eugenio Dentoni Litta, Per-Erik Hellström, Mikael Östling
KTH Royal Institute of Technology, Sweden

14:40 **STI and eSiGe Source/Drain Epitaxy Induced Stress Modeling in 28 nm Technology with Replacement Gate (RMG) Process**
Doyoung Jang, Marie Garcia Bardon, Dmitry Yakimets, Kenichi Miyaguchi, An De Keersgieter, Thomas Chiarella, Romain Ritzenthaler, Morin Dehan, Abdelkarim Mercha
Imec, Belgium

Wednesday, September 18

Emerging Memories I

Session Code: B4L-C
Location: Room C
Date & Time: Wednesday, September 18
14:00 - 15:50
Chair(s): Andrea L. Lacaita
Politecnico di Milano
Dimitris Tsoukalas
National Technical University of Athens

14:00 **Connecting RRAM Performance to the Properties of the Hafnia-Based Dielectrics (Invited Paper)**
Gennadi Bersuker[1], Brian Butcher[1], David Gilmer[1], Paul Kirsch[1], Luca Larcher[2], Andrea Padovani[2]
[1]SEMATECH, Inc., United States; [2]Università di Modena e Reggio Emilia, Italy

14:30 **Random Telegraph Noise Analysis to Investigate the Properties of Active Traps of HfO2-Based RRAM in HRS**
Francesco Maria Puglisi, Paolo Pavan, Andrea Padovani, Luca Larcher
Università di Modena e Reggio Emilia, Italy

14:50 **On the Forming-Free Operation of HfOx Based RRAM Devices: Experiments and Ab Initio Calculations**
Boubacar Traoré[1], Elisa Vianello[1], Gabriel Molas[1], Marc Gely[1], Jean François Nodin[1], Eric Jalaguier[1], Philippe Blaise[1], Barbara De Salvo[1], Kanhao Xue[2], Leonardo Fonseca[4], Yoshio Nishi[3]
[1]CEA-LETI, France; [2]IMEP-LAHC, France; [3]Stanford University, United States; [4]Universidade Estadual de Campinas, Brazil

15:10 **Weibull Analysis of the Kinetics of Resistive Switches Based on Tantalum Oxide Thin Films**
Yoshifumi Nishi, Sebastian Schmelzer, Ulrich Böttger, Rainer Waser
Rheinisch-Westfälische Technische Hochschule Aachen, Germany

15:30 **A Two-Step Set Operation for Highly Uniform Resistive Swtiching ReRAM by Controllable Filament**
Sangheon Lee, Daeseok Lee, Jiyong Woo, Euijun Cha, Hyunsang Hwang
Pohang University of Science and Technology, Korea, South

Wednesday, September 18

Reliability Aspects from Device to Circuit I

Session Code: B4L-D

Location: Room D

Date & Time: Wednesday, September 18
14:00 - 15:00

Chair(s): Paolo Pavan
University of Modena and Reggio Emilia

14:00 **ACE: a Robust Variability and Aging Sensor for High-k/Metal Gate SoC**
Min Chen[2], Vijay Reddy[2], Srikanth Krishnan[2], Jay Ondrusek[2], Yu Cao[1]
[1]Arizona State University, United States; [2]Texas Instruments, United States

14:20 **Investigation of SRAM Using BTI-Aware Statistical Compact Models**
Jie Ding[2], Dave Reid[1], Campbell Millar[1], Asen Asenov[2]
[1]Gold Standard Simulations Ltd., United Kingdom; [2]University of Glasgow, United Kingdom

14:40 **Impact of Al2O3 Position on Performances and Reliability in High-K Metal Gated DRAM Periphery Transistors**
Marc Aoulaiche[1], Eddy Simoen[1], Romain Ritzenthaler[1], Tom Schram[1], Hiroaki Arimura[1], Moonju Cho[1], Thomas Kauerauf[1], Guido Groeseneken[1], Naoto Horiguchi[1], Aaron Thean[1], Antonio Federico[5], Felice Crupi[5], Alessio Spessot[2], Christian
[1]Imec, Belgium; [2]Micron Technology Belgium, Belgium; [3]Samsung Electronics, Belgium; [4]SK-Hynix, Belgium; [5]Università della Calabria, Italy

Wednesday, September 18

Si-based Devices

Session Code: B5L-A

Location: Room A

Date & Time: Wednesday, September 18
15:00 - 16:00

Chair(s): Maryline Bawedin
Universite Montpellier 2

15:00 **Threshold Voltage Extraction Techniques and Temperature Effect in Context of Global Variability in UTBB MOSFETs**
Sergej Makovejev[2], Babak Kazemi Esfeh[2], Jean-Pierre Raskin[2], Denis Flandre[2], Valeriya Kilchytska[2], François Andrieu[1]
[1]CEA-LETI, France; [2]Université catholique de Louvain, Belgium

15:20 **Low-Temperature Transport Characteristics in SOI and sSOI Nanowires Down to 8nm Width: Evidence of IDS and Mobility Oscillations**
Rémi Coquand[2], Sylvain Barraud[1], Mikael Cassé[1], Masahiro Koyama[1], Virginie Maffini-Alvaro[1], Marie-Pierre Samson[5], Lucie Tosti[1], Xavier Mescot[3], Gerard Ghibaudo[3], Stephane Monfray[4], Frederic Boeuf[4], Olivier Faynot[1], Barbara De Salvo
[1]CEA-LETI, France; [2]CEA-LETI & STMicroelectronics & Imep-Lahc, France; [3]IMEP-LAHC, France; [4]STMicroelectronics, France; [5]STMicroelectronics & CEA, France

15:40 **Guidelines for Symmetric Threshold Voltage in Tunnel FinFETs with Single and Dual Metal Gate Electrodes**
Wataru Mizubayashi, Koichi Fukuda, Takahiro Mori, Kazuhiko Endo, Yongxun Liu, Takashi Matsukawa, Shin-Ichi O'uchi, Yuki Ishikawa, Shinji Migita, Yukinori Morita, Akihito Tanabe, Junichi Tsukada, Hiromi Yamauchi, Meishoku Masahara, Hiroyuki Ota
National Institute of Advanced Industrial Science and Technology, Japan

Wednesday, September 18

Silicon Doping

Session Code: B5L-B
Location: Room B
Date & Time: Wednesday, September 18
15:00 - 16:00
Chair(s): Emmanuel Augendre
CEA

15:00 **On the Strain Induced by Arsenic into Silicon**
Stéphane Koffel[1], Peter Pichler[2], Jürgen Lorenz[1], Gabriele Bisognin[3], Enrico Napolitani[3], Davide De Salvador[3]
[1]Fraunhofer IISB, Germany; [2]Fraunhofer IISB & Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany; [3]Università di Padova, Italy

15:20 **High-Ohmic Resistors Using Nanometer-Thin Pure-Boron Chemical-Vapour-Deposited Layers**
Negin Golshani, Vahid Mohammadi, Siva Ramesh, Lis Nanver
Technische Universiteit Delft, Netherlands

15:40 **Melt Depth and Time Variations During Pulsed Laser Thermal Annealing with One and More Pulses**
Moritz Hackenberg[3], Mathias Rommel[3], Maximilian Rumler[3], Jürgen Lorenz[3], Peter Pichler[4], Karim Huet[2], Razvan Negru[2], Giuseppe Fisicaro[1], Antonino La Magna[1], Nadjib Taleb[5], Maurice Quillec[5]
[1]CNR IMM, Italy; [2]Excico, France; [3]Fraunhofer IISB, Germany; [4]Fraunhofer IISB & Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany; [5]Probion, France

Wednesday, September 18

Reliability Aspects from Device to Circuit II

Session Code: B5L-D

Location: Room D

Date & Time: Wednesday, September 18
15:00 - 16:00

Chair(s): Paolo Pavan
University of Modena and Reggio Emilia

15:00 **Effect of Ions Presence in the SiOCH Inter Metal Dielectric Structure**
Benjamin Rebuffat[2], Vincenzo Della Marca[2], Pascal Masson[3], Jean Luc Ogier[2], Marc Mantelli[2], Olivier Paulet[2], Laurent Lopez[2], Romain Laffont[1]
[1]IM2NP, France; [2]STMicroelectronics, France; [3]Université de Nice Sophia, France

15:20 **Novel Back-Biased UTBB Lateral SCR for FDSOI ESD Protections**
Yohann Solaro[3], Pascal Fonteneau[3], Charles-Alexandre Legrand[3], Claire Fenouillet-Beranger[1], Philippe Ferrari[2], Sorin Cristoloveanu[2]
[1]CEA-LETI, France; [2]IMEP-LAHC, France; [3]STMicroelectronics, France

15:40 **Reliability Tests for Discriminating Between Technological Variants of QFN Packaging**
Marius Bâzu[2], Virgil Emil Ilian[2], Dragos Vârsescu[2], Lucian Galateanu[2], Vili Sikiö[3], Meelis Reimets[3], Volker Uhl[1], Manuel Weiss[1]
[1]Austrian Research Institute for Chemistry and Technology, Austria; [2]IMT Bucharest, Romania; [3]Pera Technology, Estonia

Wednesday, September 18

Emerging MOS: Variability & Defects

Session Code: B6L-A
Location: Room A
Date & Time: Wednesday, September 18
16:30 - 17:50
Chair(s): Tibor Grasser
TU Wien
Ray Hueting
Universiteit Twente

16:30 **Multi-Scale Computational Framework for the Evaluation of Variability in the Programing Window of a Flash Cell with Molecular Storage**
Vihar Georgiev[1], Stanislav Markov[2], Laia Vilà-Nadal[1], Cristoph Busche[1], Leroy Cronin[1], Asen Asenov[1]
[1]University of Glasgow, United Kingdom; [2]University of Honk Kong, China

16:50 **Impact of Statistical Variability and Charge Trapping on 14 nm SOI FinFET SRAM Cell Stability**
Xingsheng Wang[3], Binjie Cheng[3], Andrew Brown[1], Campbell Millar[1], Jente B. Kuang[2], Sani Nassif[2], Asen Asenov[3]
[1]Gold Standard Simulations Ltd., United Kingdom; [2]IBM Austin Research Lab, United States; [3]University of Glasgow, United Kingdom

17:10 **Flicker Noise in Advanced CMOS Technology: Effects of Halo Implant**
Navid Paydavosi[2], Sriramkumar Venugopalan[2], Angada Sachid[2], Ali Niknejad[2], Chenming Hu[2], Sagnik Dey[1], Samuel Martin[1], Xin Zhang[1]
[1]Texas Instruments, United States; [2]University of California, Berkeley, United States

17:30 **Characterization of N-Channel 4H-SiC MOSFETs: Electrical Measurements and Simulation Analysis**
Viktoryia Uhnevionak[1], Christian Strenger[1], Alex Burenkov[1], V. Mortet[3], E. Bedel-Pereira[3], Jürgen Lorenz[1], Peter Pichler[2]
[1]Fraunhofer IISB, Germany; [2]Fraunhofer IISB & Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany; [3]LAAS-CNRS & Wide Bandgap Semiconductor Alliance, France

Wednesday, September 18

Nanowire Electronics

Session Code: B6L-B
Location: Room B
Date & Time: Wednesday, September 18
16:30 - 17:40
Chair(s): Costin Anghel
ISEP
Elena Gnani
University of Bologna

16:30 **Reconfigurable Nanowire Electronics - Device Principles and Circuit Prospects (Invited Paper)**
Walter M. Weber, Jens Trommer, Dominik Martin, Matthias Grube, André Heinzig, Thomas Mikolajick
Namlab gGmbH & Technische Universität Dresden, Germany

17:00 **Electrical and Thermoelectrical Properties of Gated InAs Nanowires**
Philipp Mensch, Siegfried Karg, Bernd Gotsmann, Pratyush Das Kanungo, Volker Schmidt, Valentina Troncale, Heinz Schmid, Heike Riel
IBM Research GmbH, Switzerland

17:20 **Low Frequency Noise in Strained Silicon Nanowire Array MOSFETs and Tunnel-FETs**
Simon Richter[1], Svetlana Vitusevich[1], Sergii Pud[1], Jing Li[1], Lars Knoll[1], Stefan Trellenkamp[1], Anna Schäfer[1], Steffi Lenk[1], Qing-Tai Zhao[1], Andreas Offenhäusser[1], Siegfried Mantl[1], Konstantin Bourdelle[2]
[1]Peter-Grünberg-Institut, Germany; [2]SOITEC, France

Wednesday, September 18

Emerging Memories II

Session Code: B6L-C
Location: Room C
Date & Time: Wednesday, September 18
16:30 - 17:30
Chair(s): Kazunari Ishimaru
Toshiba Corp.
Olivier Thomas
CEA-LETI

16:30 **Strontium Doped Hafnium Oxide Thin Films: Wide Process Window for Ferroelectric Memories**
Tony Schenk[3], Stefan Mueller[3], Uwe Schroeder[3], Robin Materlik[1], Alfred Kersch[1], Mihaela Popovici[2], Christoph Adelmann[2], Sven Van Elshocht[2], Thomas Mikolajick[3]
[1]Hochschule für angewandte Wissenschaften, Germany; [2]Imec, Belgium; [3]Namlab gGmbH & Technische Universität Dresden, Germany

16:50 **A Novel HfO2-GeS2-Ag Based Conductive Bridge Ram for Reconfigurable Logic Applications**
Giorgio Palma, Elisa Vianello, Olivier Thomas, Houcine Oucheikh, Santhosh Onkaraiah, Alain Toffoli, Catherine Carabasse, Gabriel Molas, Barbara De Salvo
CEA-LETI, France

17:10 **Nonvolatile Resistive Memory Devices Based on Hydrogenated Amorphous Carbon**
Laurent Dellmann, Abu Sebastian, Vara Prasad Jonnalagadda, Claudia Santini, Wabe Koelmans, Christophe Rossel, Evangelos Eleftheriou
IBM Research GmbH, Switzerland

Thursday, September 19

More than Moore

Session Code: C3L-A
Location: Room A
Date & Time: Thursday, September 19
11:20 - 12:20
Chair(s): Steve Hall
University of Liverpool
Ryoichi Ishihara
TU Delft

11:20 **Monolithic Integration of Pseudo-Spin-MOSFETs Using a Custom CMOS Chip Fabricated Through Multi-Project Wafer Service**
Ryosho Nakane[3], Yusuke Shuto[2], Hiroaki Sukegawa[1], Zhenchao Wen[1], Shuu'Ichirou Yamamoto[2], Seiji Mitani[1], Masaaki Tanaka[3], Koichiro Inomata[1], Satoshi Sugahara[2]
[1]National Institute for Materials Science, Japan; [2]Tokyo Institute of Technology, Japan; [3]University of Tokyo, Japan

11:40 **Nanomagnetic Logic Clocked in the MHz Regime**
Markus Becherer[1], Josef Kiermaier[1], Stephan Breitkreutz[1], Irina Eichwald[1], György Csaba[2], Doris Schmitt-Landsiedel[1]
[1]Technische Universität München, Germany; [2]University of Notre Dame, United States

12:00 **Micron-Scale Inkjet-Assisted Digital Lithography for Large-Area Flexible Electronics**
Radu Sporea, Abdullah Alshammari, Stamatis Georgakopoulos, John Underwood, Maxim Shkunov, Ravi Silva
University of Surrey, United Kingdom

Thursday, September 19

MEMS Devices and Technologies I

Session Code: C3L-B

Location: Room B

Date & Time: Thursday, September 19
11:20 - 12:20

Chair(s): Mart Graef
TU Delft

11:20 **Design and Array Implementation a Cantilever-Based Non-Volatile Memory Utilizing Vibrational Reset**
Anh Tuan Do[2], Jayaraman Karthik Gopal[2], Pushpapraj Singh[1], Chua Geng Li[1], Kiat Seng Yeo[2], Tony Tae-Hyoung Kim[2]
[1]Institute of Microelectronics, Singapore; [2]Nanyang Technological University, Singapore

11:40 **RF MEMS Power Sensors for Ultra-Low Power Wake-Up Circuit Applications**
Wolfgang Vitale, Montserrat Fernández-Bolaños, Antonios Bazigos, Catherine Dehollain, Adrian Mihai Ionescu
École Polytechnique Fédérale de Lausanne, Switzerland

12:00 **Design of a Poly Silicon MEMS Microphone for High Signal-to-Noise Ratio**
Alfons Dehé, Martin Wurzer, Marc Füldner, Ulrich Krumbein
Infineon Technologies AG, Germany

Thursday, September 19

Advanced Characterization of Novel MOS FET Structures

Session Code: C3L-D

Location: Room D

Date & Time: Thursday, September 19
11:20 - 12:20

Chair(s): Henryk Przewlocki
Institute of Electron Technology
Gunnar Malm
KTH Royal Institute of Technology

11:20 **Magnetoresistance Measurements and Unusual Mobilitiy Behavior in FD MOSFETs**
Sung-Jae Chang[2], Sorin Cristoloveanu[2], Maryline Bawedin[4], Jong-Hyun Lee[3], Jung-Hee Lee[3], Sutirtha Mukhopadhyay[1], Benjamin A. Piot[1]
[1]Grenoble High Magnetic Field Laboratory, CNRS, France; [2]IMEP-LAHC, France; [3]Kyungpook National University, Korea, South; [4]Université de Montpellier 2, France

11:40 **Influence of Device Scaling on Low-Frequency Noise in SOI Tri-Gate N- and P-Type Si Nanowire MOSFETs**
Masahiro Koyama[1], Mikaël Cassé[1], Rémi Coquand[2], Sylvain Barraud[1], Gérard Ghibaudo[3], Hiroshi Iwai[4], Gilles Reimbold[1]
[1]CEA-LETI, France; [2]CEA-LETI & STMicroelectronics & Imep-Lahc, France; [3]IMEP-LAHC, France; [4]Tokyo Institute of Technology, Japan

12:00 **Why Are SCE Overestimated in FD-SOI MOSFETs?**
Carlos Navarro Moral[4], Maryline Bawedin[3], François Andrieu[1], Bruno Sagnes[3], Sorin Cristoloveanu[2]
[1]CEA-LETI, France; [2]IMEP-LAHC, France; [3]Université de Montpellier 2, France; [4]Université de Montpellier 2 & IMEP-LAHC, France

ESSDERC Technical Program

Thursday, September 19

ESSDERC Keynote: K. Banerjee (UC, Santa Barbara)

Session Code: C4L-E

Location: Room CT

Date & Time: Thursday, September 19
14:00 - 15:00

Chair(s): Max Lemme
University of Siegen

14:00 **2D Electronics: Graphene and Beyond**
Kaustav Banerjee, Wei Cao, Jiahao Kang, Wei Liu, Yasin Khatami, Deblina Sarkar
University of California, Santa Barbara, United States

Thursday, September 19

ESSDERC Invited Session II

Session Code: C5L-E

Location: Room CT

Date & Time: Thursday, September 19
15:00 - 16:00

Chair(s): Gheorghe Brezeanu
Politehnica University Bucharest

15:00 **Atomistic Simulation of Electron and Phonon Transport in Nano-Devices**
Mathieu Luisier, Reto Rhyner
ETH Zürich, Switzerland

Thursday, September 19

Carbon-based Devices

Session Code: C6L-D
Location: Room D
Date & Time: Thursday, September 19
16:20 - 17:40
Chair(s): Adrian Ionescu
EPFL
Mircea Dragoman
IMT Bucharest

16:20 **DC and Small-Signal Numerical Simulation of Graphene Base Transistor for Terahertz Operation**
Valerio Di Lecce[2], Roberto Grassi[1], Antonio Gnudi[1], Elena Gnani[1], Susanna Reggiani[1], Giorgio Baccarani[1]
[1]Università di Bologna, Italy; [2]University of Bologna, Italy

16:40 **Graphene-Channel FETs for Photonic Frequency Double-Mixing Conversion Over the Sub-THz Band**
Tetsuya Kawasaki[2], Adrian Dobroiu[2], Takanori Eto[2], Yuki Kurita[2], Kazuki Kojima[2], Yuhei Yabe[2], Hiroki Sugiyama[2], Takayuki Watanabe[2], Susumu Takabayashi[2], Tetsuya Suemitsu[2], Victor Ryzhii[2], Katsumi Iwatsuki[2], Taiichi Otsuji[2], Youic
[1]Nippon Telegraph and Telephone Corporation, Japan; [2]Tohoku University, Japan

17:00 **On-Wafer Graphene Diodes for High-Frequency Applications**
Mircea Dragoman[1], Adrian Dinescu[1], Daniela Dragoman[2]
[1]IMT Bucharest, Romania; [2]University of Bucharest, Romania

17:20 **Carbon Nanotube Resistors as Gas Sensors: Towards Selective Analyte Detection with Various Metal-Nanotube Interfaces**
Hoël Guerin[2], Hélène Le Poche[1], Roland Pohle[3], Montserrat Fernández-Bolaños[2], Jean Dijon[1], Adrian Mihai Ionescu[2]
[1]Commissariat à l'énergie atomique et aux énergies alternatives, France; [2]École Polytechnique Fédérale de Lausanne, Switzerland; [3]SIEMENS AG Corporate Research, Germany

Thursday, September 19

Emerging Memory Modeling

Session Code: C6L-E
Location: Room CT
Date & Time: Thursday, September 19
16:20 - 18:00
Chair(s): Cristell Maneux
IMS
An De Keetsgieter
IMEC

16:20 **A Negative Differential Resistance Effect Implemented with a Single MOSFET from 375 K Down to 80 K**
Victor Vega-González[2], Edmundo Gutiérrez-Domínguez[2], Fernando Guarin[1]
[1]IBM Microelectronics, United States; [2]Instituto Nacional de Astrofísica, Óptica y Electrónica, Mexico

16:40 **Reduction of Momentum and Spin Relaxation Rate in Strained Thin Silicon Films**
Dmitry Osintsev, Viktor Sverdlov, Siegfried Selberherr
Technische Universität Wien, Austria

17:00 **Compact Modeling of STT-MTJ for SPICE Simulation**
Zihan Xu, Ketul Sutaria, Chengen Yang, Chaitali Chakrabarti, Yu Cao
Arizona State University, United States

17:20 **Understanding the Conduction Mechanism of the Chalcogenide Ag2S Silver-Doped Through Ab Initio Simulation**
Tsanka Todorova[1], Philippe Blaise[1], Elisa Vianello[1], Leonardo Fonseca[2]
[1]CEA-LETI, France; [2]Universidade Estadual de Campinas, Brazil

17:40 **Modeling the Dynamic Self-Heating of PCM**
Giuliano Marcolini[1], Fabio Giovanardi[1], Massimo Rudan[1], Fabrizio Buscemi[1], Enrico Piccinini[1], Rossella Brunetti[2], Andrea Cappelli[2]
[1]Università di Bologna, Italy; [2]Università di Modena e Reggio Emilia, Italy

Thursday, September 19

MEMS Devices and Technologies II

Session Code: C6L-F
Location: Room TM
Date & Time: Thursday, September 19
16:20 - 17:40
Chair(s): Piotr Grabiec
Instytut Technologii Elektronowej ITE

16:20 **Low Power FinFET pH-Sensor with High-Sensitivity Voltage Readout**
Sara Rigante[1], Paolo Livi[2], Mathias Wipf[4], Kristine Bedner[3], Didier Bouvet[1], Antonios Bazigos[1], Alexandru Rusu[5], Andreas Hierlemann[2], Adrian Mihai Ionescu[1]
[1]École Polytechnique Fédérale de Lausanne, Switzerland; [2]ETH Zürich, Switzerland; [3]Paul Scherrer Institute, Switzerland; [4]Universität Basel, Switzerland; [5]Universitatea Politehnica din Bucuresti, Romania

16:40 **Flexible Platinum Nanoparticle Strain Sensors**
Evangelos Skotadis[1], Dimitris Mousadakos[1], Joseph Tanner[1], Dimitris Tsoukalas[1], Panagiotis Broutas[2]
[1]National Technical University of Athens, Greece; [2]NCSR Demokritos, Greece

17:00 **MEMS Sensors for High Voltage Lines**
Victor Moagar-Poladian, Gabriel Moagar-Poladian
National Institute for Research and Development in Microtechnology, Romania

17:20 **Investigation of Gate Material Ductility Enables Flexible a-IGZO TFTs Bendable to a Radius of 1.7 mm**
Niko Münzenrieder, Luisa Petti, Christoph Zysset, Deniz Görk, Lars Büthe, Giovanni Salvatore, Gerhard Tröster
ETH Zürich, Switzerland

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