Boosting InAs TFET on-current above 1 mA/μm with no leakage penalty

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Outline

- Introduction and motivation
- Design guidelines of the TFET optimization approach
- I_{ON} boosting
- Reducing I_{OFF} without affecting I_{ON}
- Optimized design
  - ❖ Benchmark: ITRS specs of multi-gate transistors (2020)
- Conclusions

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Introduction & Motivation

- MOSFET

  Charge injection by thermionic emission over a potential barrier →

  ☹ best inverse subthreshold slope (SS) 60 mV/dec

- Tunnel-Field-Effect Transistor (TFET)

  Charge injection by Band-to-Band-Tunneling (BTBT) →

  ☺ SS can be reduced below 60 mV/dec

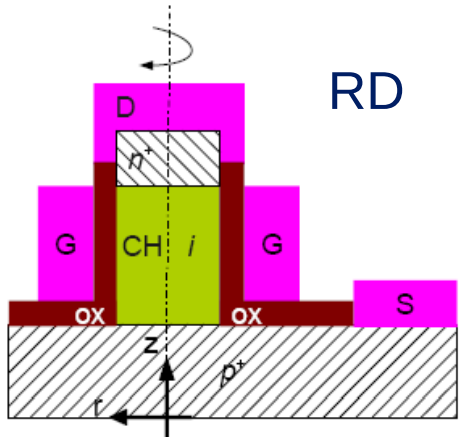
  ☹ Sub-thermal slopes difficult to be maintained for many I_{DS}-decades

  ☹ I_{ON} is generally too low (<< 1mA/μm) especially using Si

[Seabaugh, Zhang, Proc.IEEE,2010]

➢ Propose a TFET able to provide I_{ON} > 1mA/μm at lower supply voltage (V_{DD}) compared to the ITRS, while targeting HP and LOP specs in terms of I_{OFF}

Reference Device (RD) and TCAD model



- RD (starting point of TCAD optimization):

  cylindrical vertical GAA InAs NW *n*-TFET (ϕ= 20 nm)

- Increase tunneling probability for high I_{ON}:
  - low band-gap, low effective mass → InAs
  - High-field → doping steepness of 1nm/dec

$$T_{WKB} = e^{\left[-\frac{4\sqrt{2m^*}(E_G+E_\perp)^{3/2}}{3\,q\,\hbar\,\mathcal{E}}\right]}$$

[Seabaugh, Zhang,Proc.IEEE,2010]

- Enhance electrostatic control:
  - High-k (Al_2O_3) and metal gate; EOT aligned with LOP specs
- High I_{ON}, low I_{OFF}:
  - *p*-type source more doped than *n*-type drain ($5x10^{19}cm^{-3}$ vs. $5x10^{18}cm^{-3}$)

- Channel 40 nm →TCAD model: drift-diffusion
  - BTBT treated as carrier generation mechanism [Kane,JAP,1961]
  - Doping dependent mobility model for InAs [Sootodeh,et al.,JAP,2000]

- V_{DD} = 0.5 V

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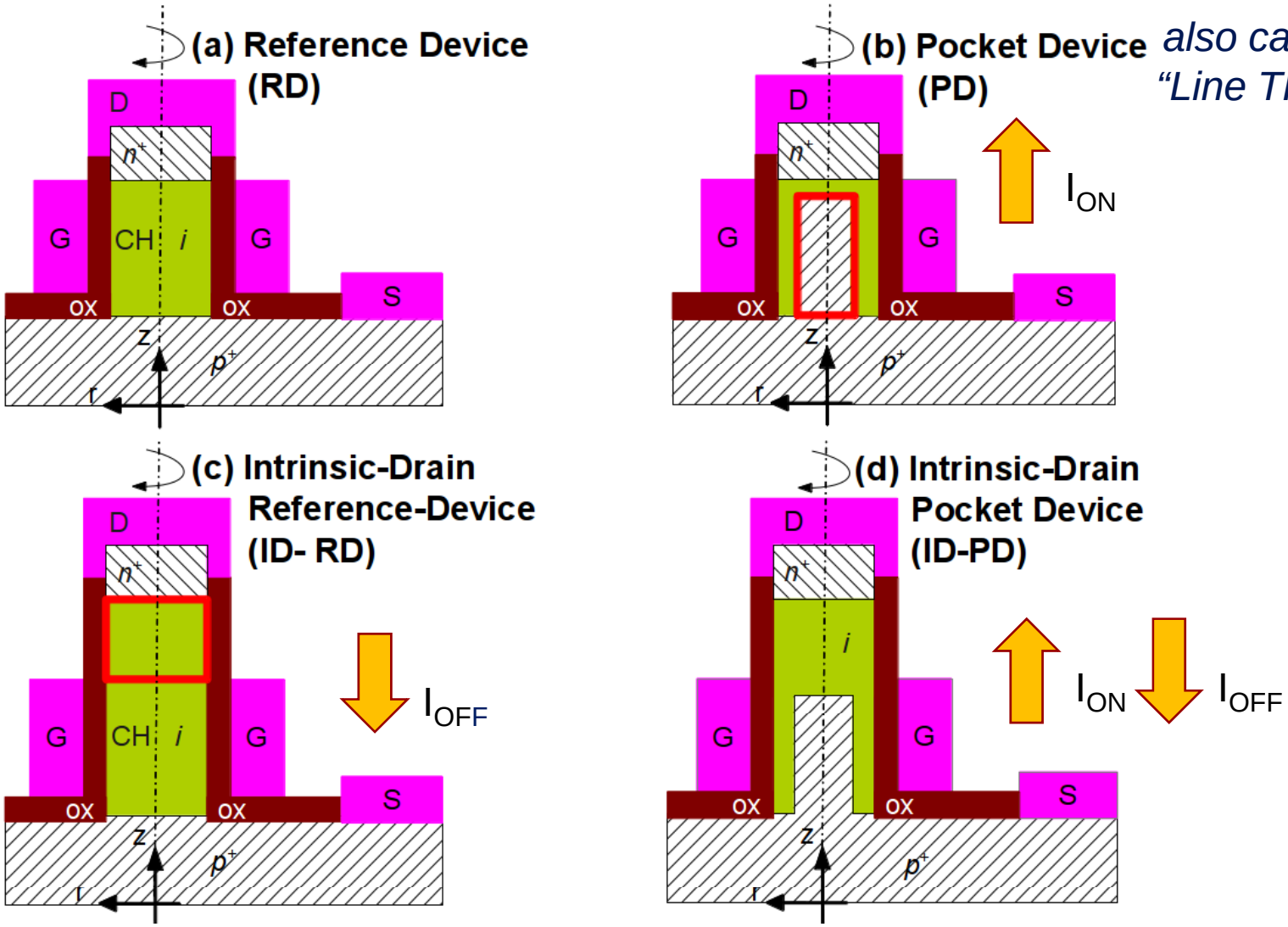
Cross-sections of TFET proposed in this work



optimized ID-PD fulfills HP and LOP 2020 ITRS specs at lower V_{DD}

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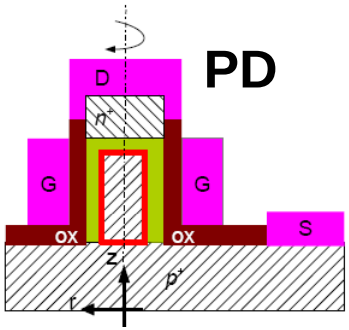
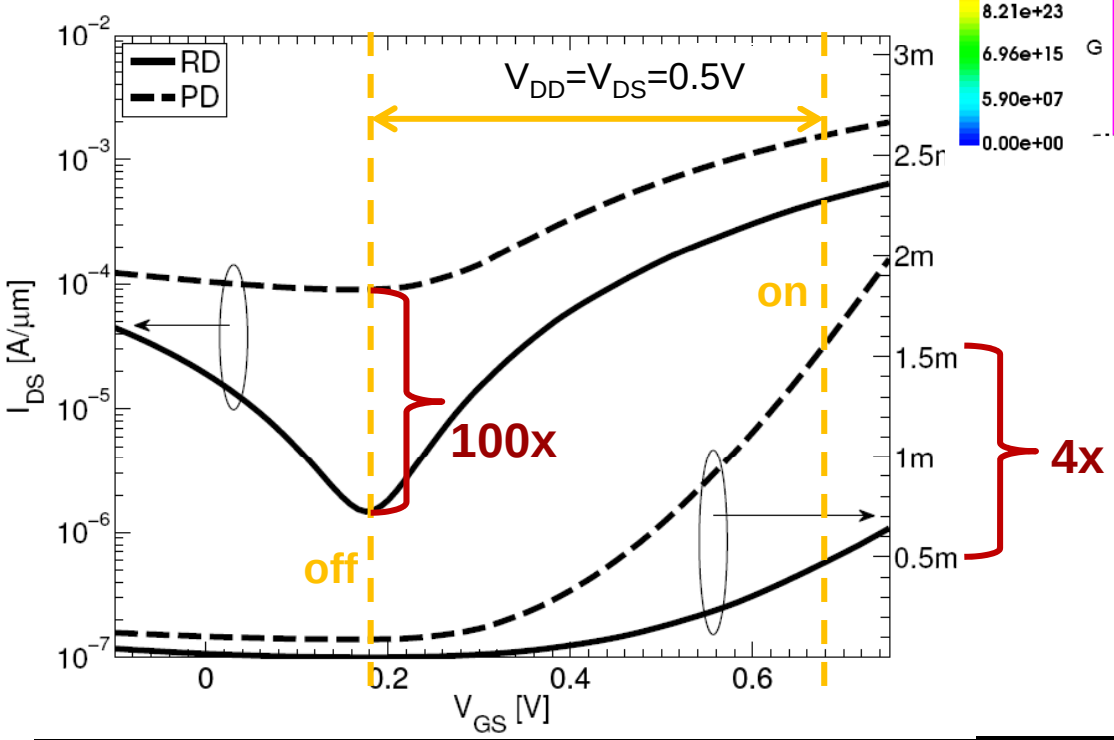
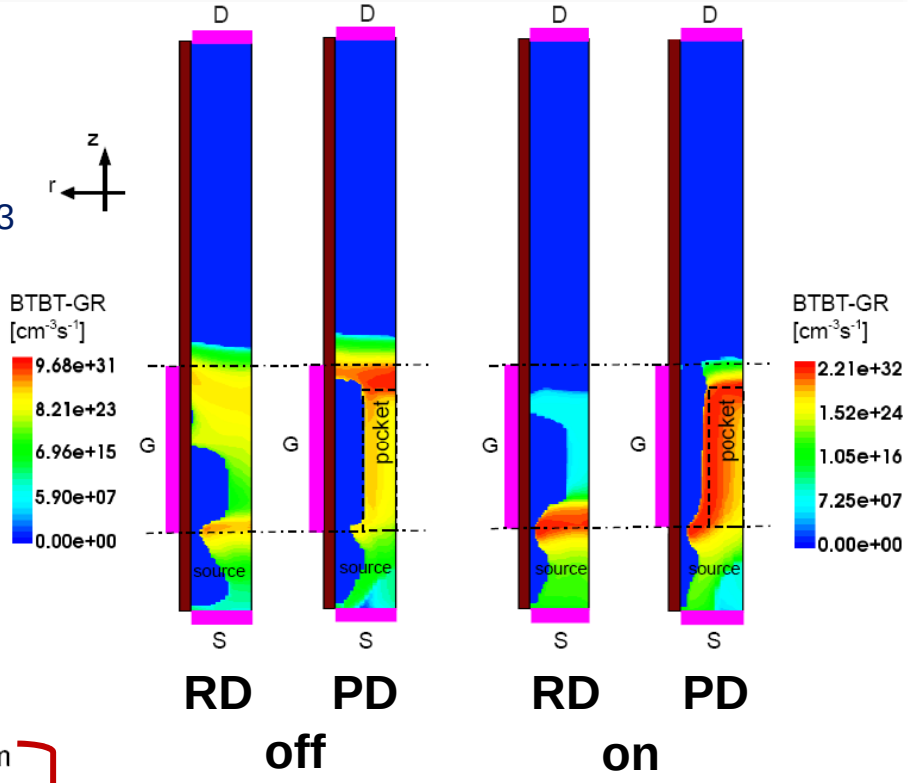
Turn-on characteristics: RD vs. PD



PD: pocket having
- 35 nm-length
- p^+ doping $5x10^{19}cm^{-3}$
- 5nm-radius



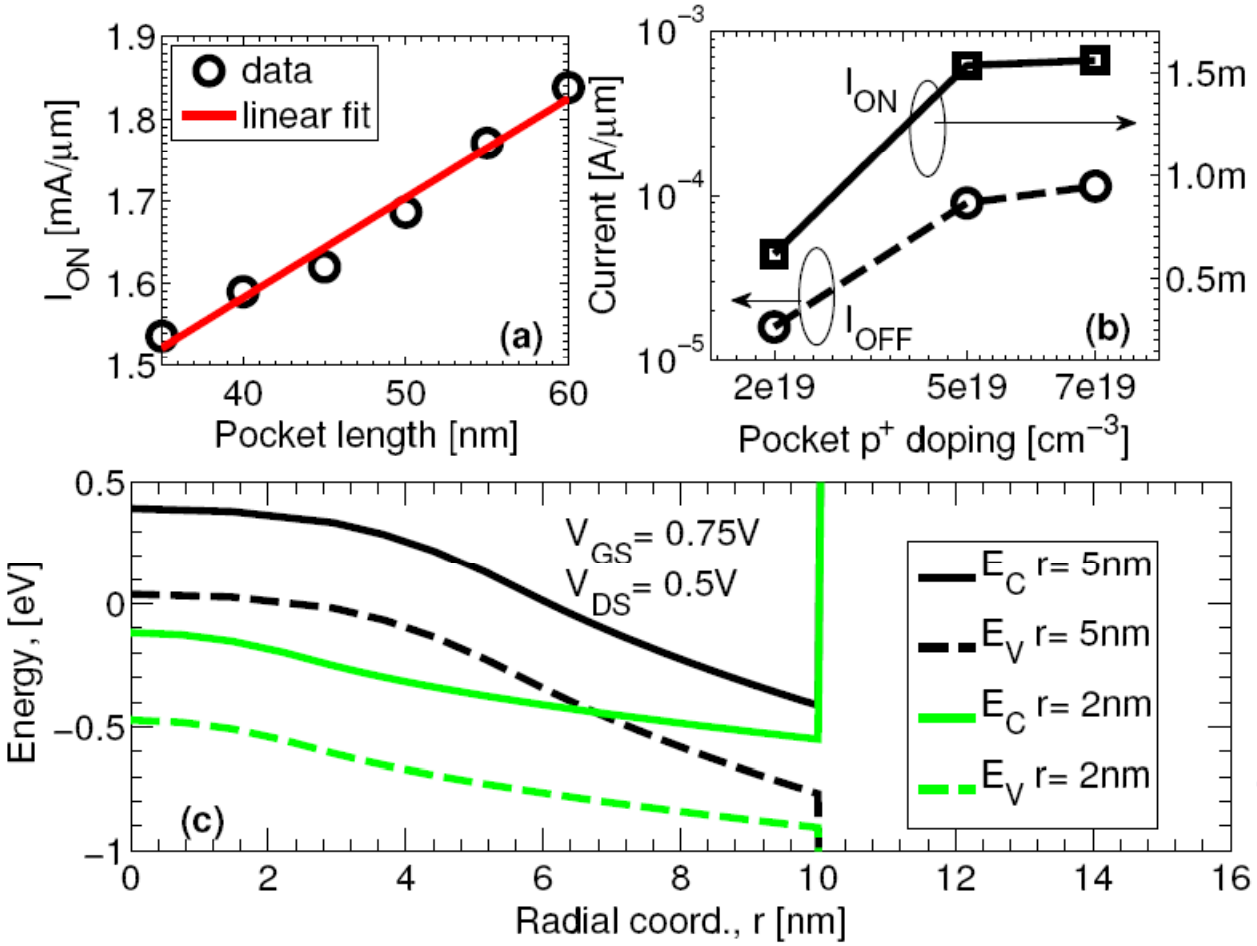


off: leakage mainly due to upper-pocket junction

off & on: good electrostatic control of pocket sidewalls

Pocket optimization

15 μA/μm/nm



Providing HP-compatible I_{ON}= 2 mA/μm requires:

- Pocket length 35 nm
- p^+ doping $7x10^{19}cm^{-3}$
- 6nm-radius
- t_{ox} aligned with HP-EOT specs

"improved pocket"

"Improved Pocket Device" (IPD)

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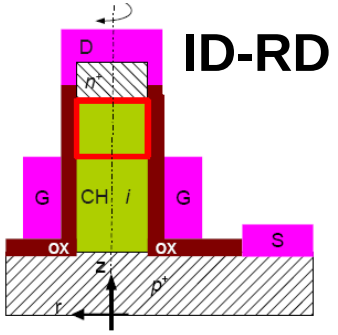
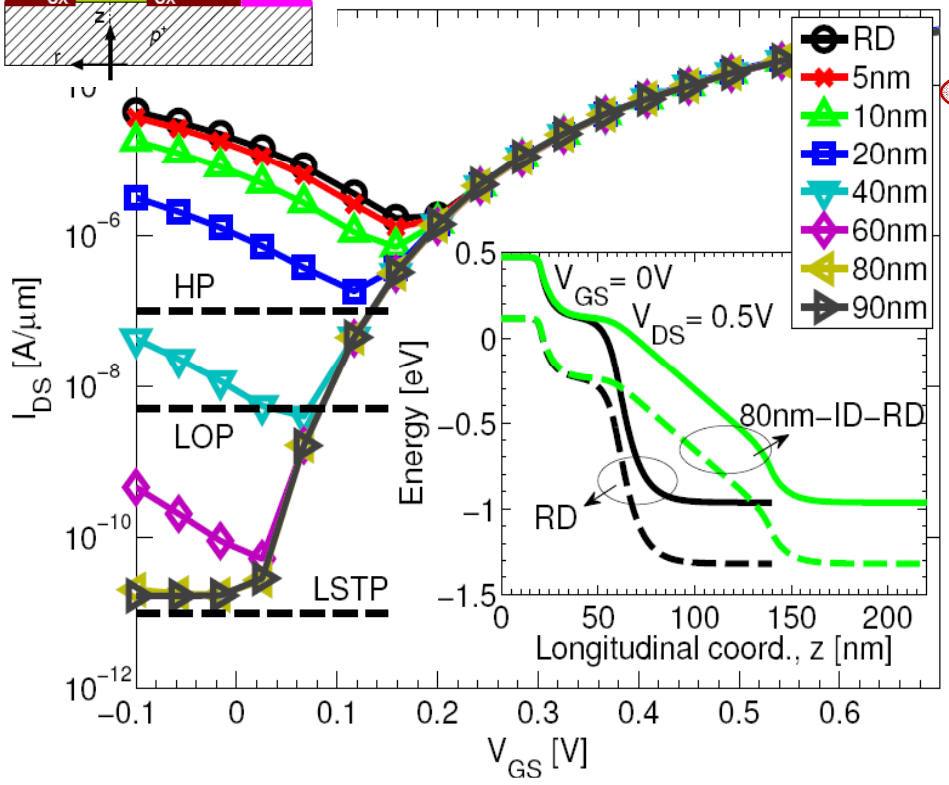
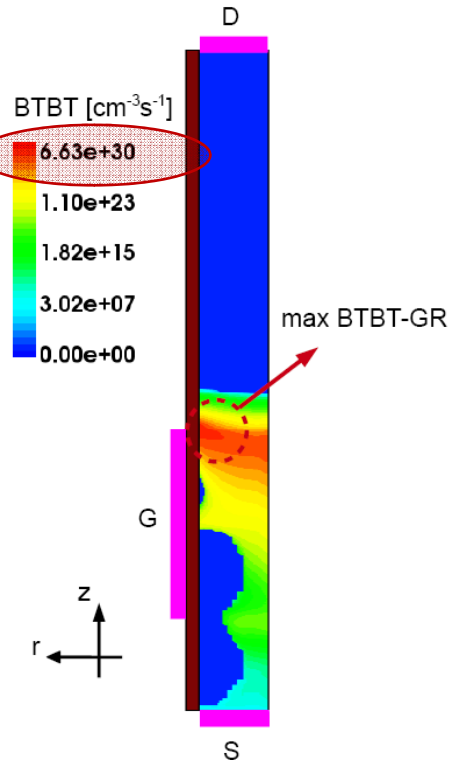
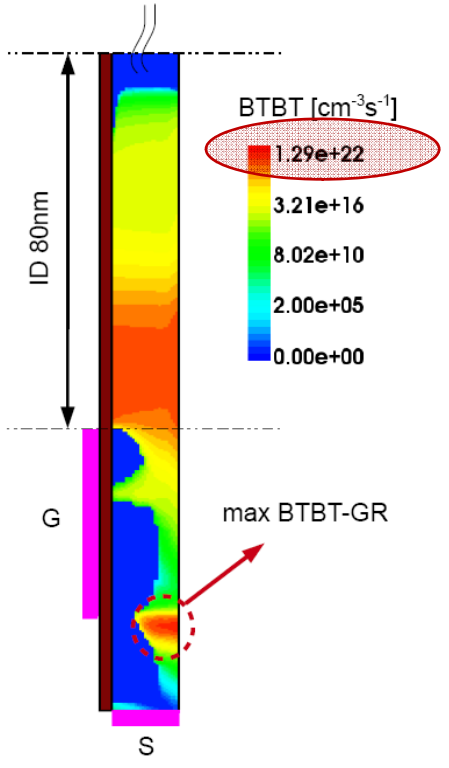
Turn-on of ID-RD varying ID length









RD **80nm-ID**

V_{GS}=0V, V_{DS}=0.5V

- I_{ON}/I_{OFF} increased of 5 orders of magnitude from RD to 80nm-ID-RD
- A sufficiently long ID completely suppresses TFET ambipolarity

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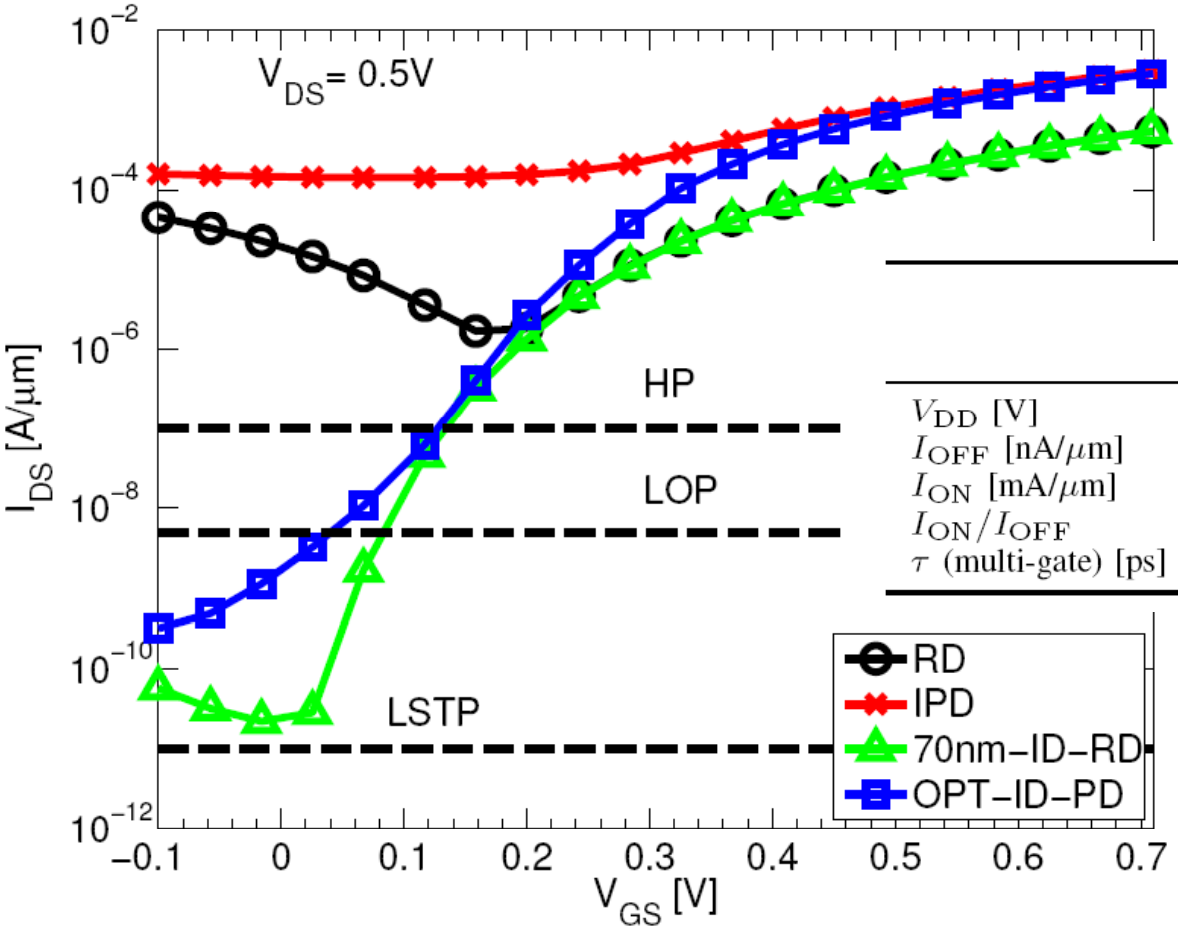
✓ ***Optimized design***

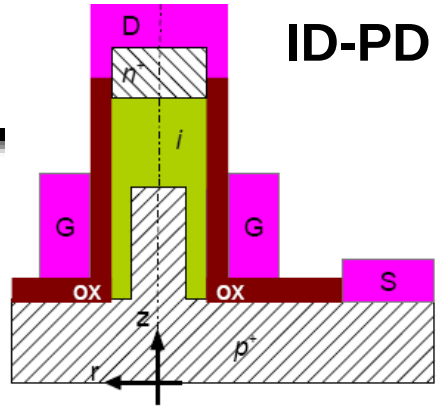
  ❖ Benchmark: ITRS specs of multi-gate transistors (2020)

- Conclusions.

OPT-ID-PD turn-on characteristics



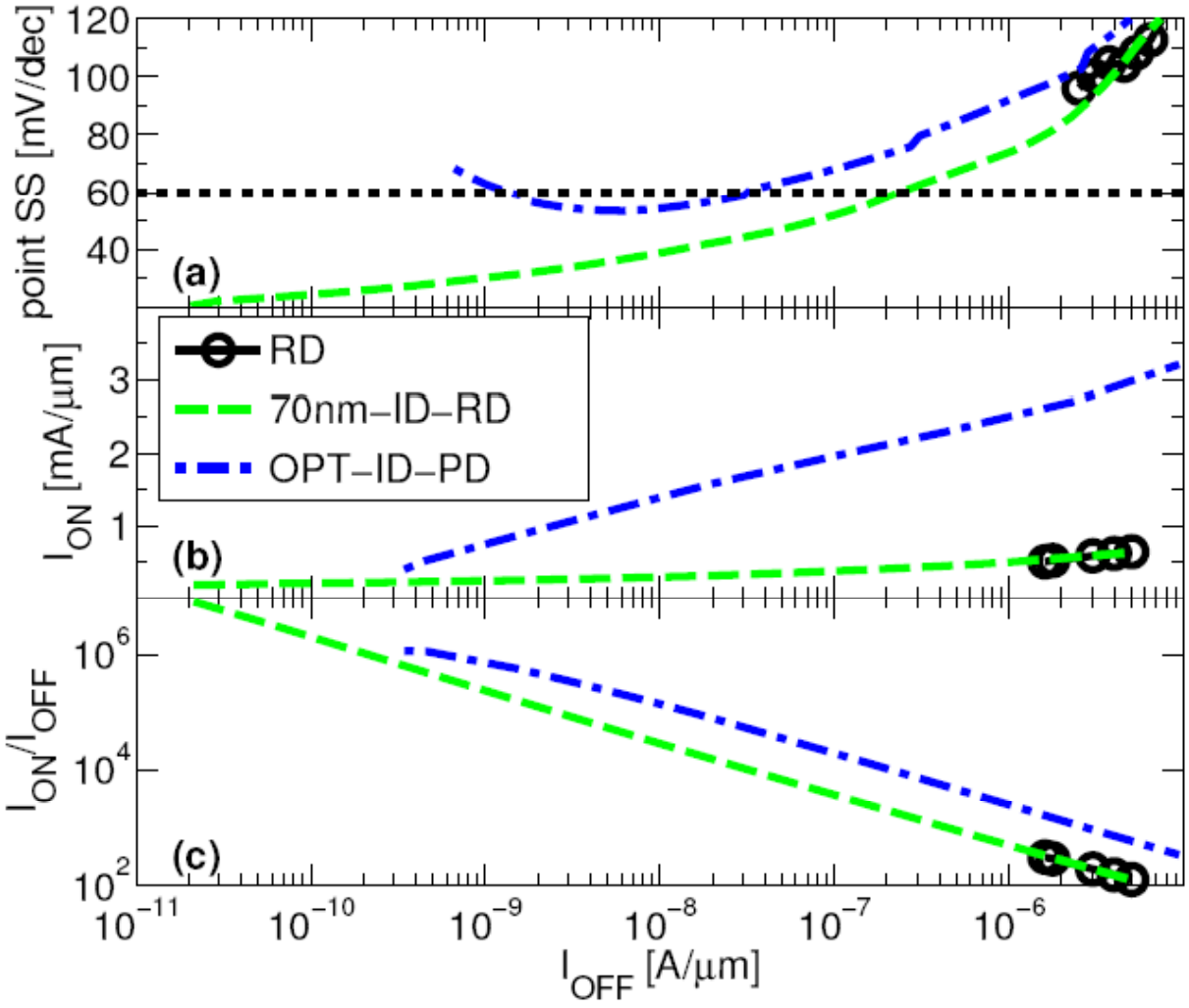
ID-PD



	OPT-ID-PD		ITRS (2020)	
	LOP	HP	LOP	HP
V_{DD} [V]	0.5	0.5	0.53	0.68
I_{OFF} [nA/μm]	5	100	5	100
I_{ON} [mA/μm]	1.119	1.978	0.784	1.916
I_{ON}/I_{OFF}	~2.4e5	~2.0e4	~1.5e5	~1.9e4
τ (multi-gate) [ps]	0.82	0.44	0.35	0.19

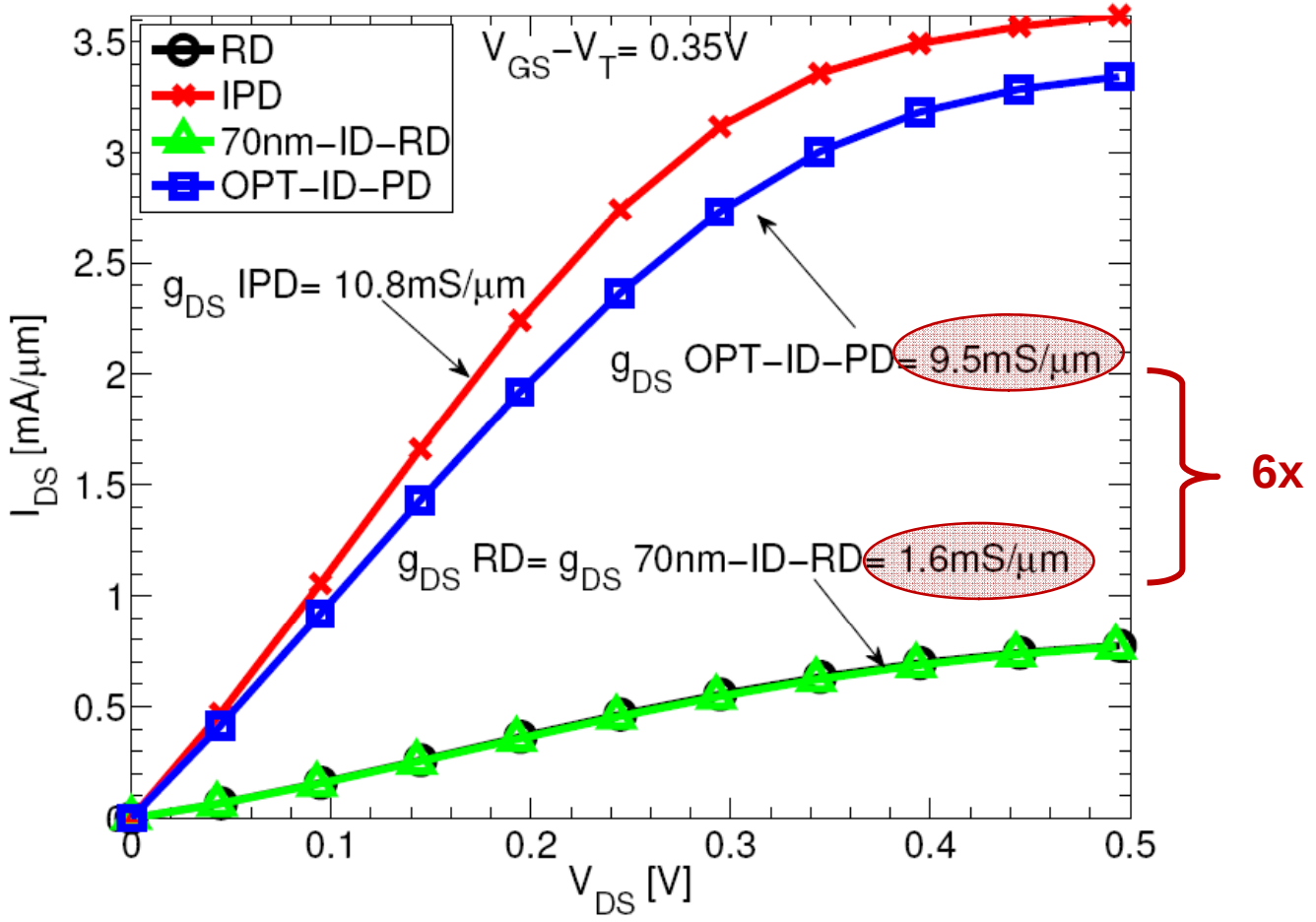
OPT-ID-PD fulfills both HP and LOP current specs at reduced V_{DD} yielding 25% of reduction of static power for the HP case

OPT-ID-PD: additional information



- Point SS below 60mV/dec within about 1 I_{DS}-order
- I_{ON} ~ 2 mA/μm highest value reported in literature for TFET simulated at ITRS-compliant V_{DD}
- Max $I_{ON}/I_{OFF} > 10^6$

Output characteristics



Output conductance g_{DS} of OPT-ID-PD ~6x RD g_{DS} thanks to pocket
→ key factor for TFET rail-to-rail logic switching [Pal, IEEE T-ED, 2011]

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Conclusions and perspectives

➢ Conclusions:

- A TFET featuring I_{ON} in the mA/μm range has been proposed for the first time
- Design & optimization by means of TCAD simulations
  →integration of pocket & intrinsic drain for both high I_{ON} and low I_{OFF}
- Optimized TFET fulfills I_{ON} and I_{OFF} 2020 HP and LOP ITRS specs for multi-gate transistors at V_{DD} = 0.5 V
  → 25% reduction in static power consumption (HP specs)

➢ Perspectives:

- Further optimization to fulfill LSTP off specs as well and reduce SS
  → achieved by splitting the gate into a Dual-Metal-Gate

G. Betti Beneventi, et al., submitted to IEEE T-ED

Acknowledgments

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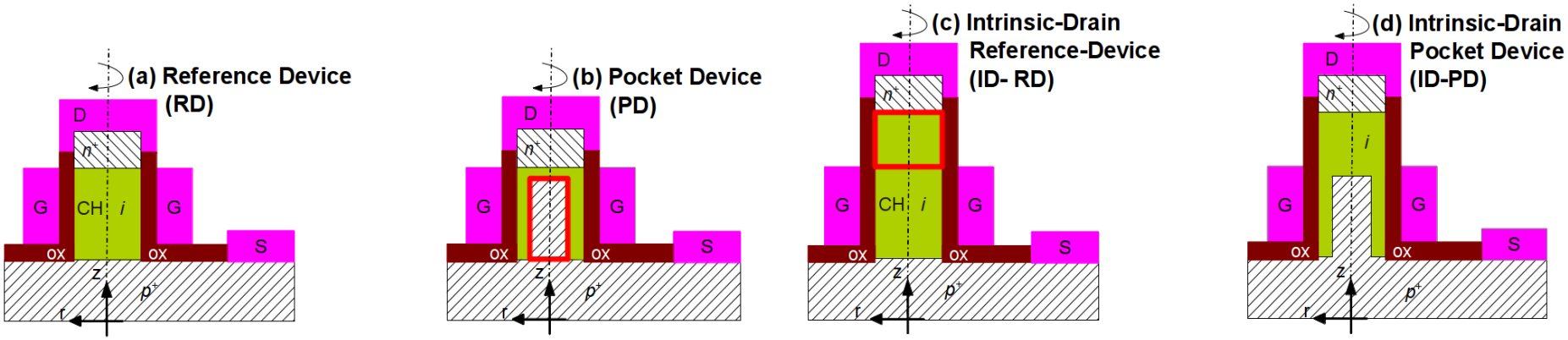
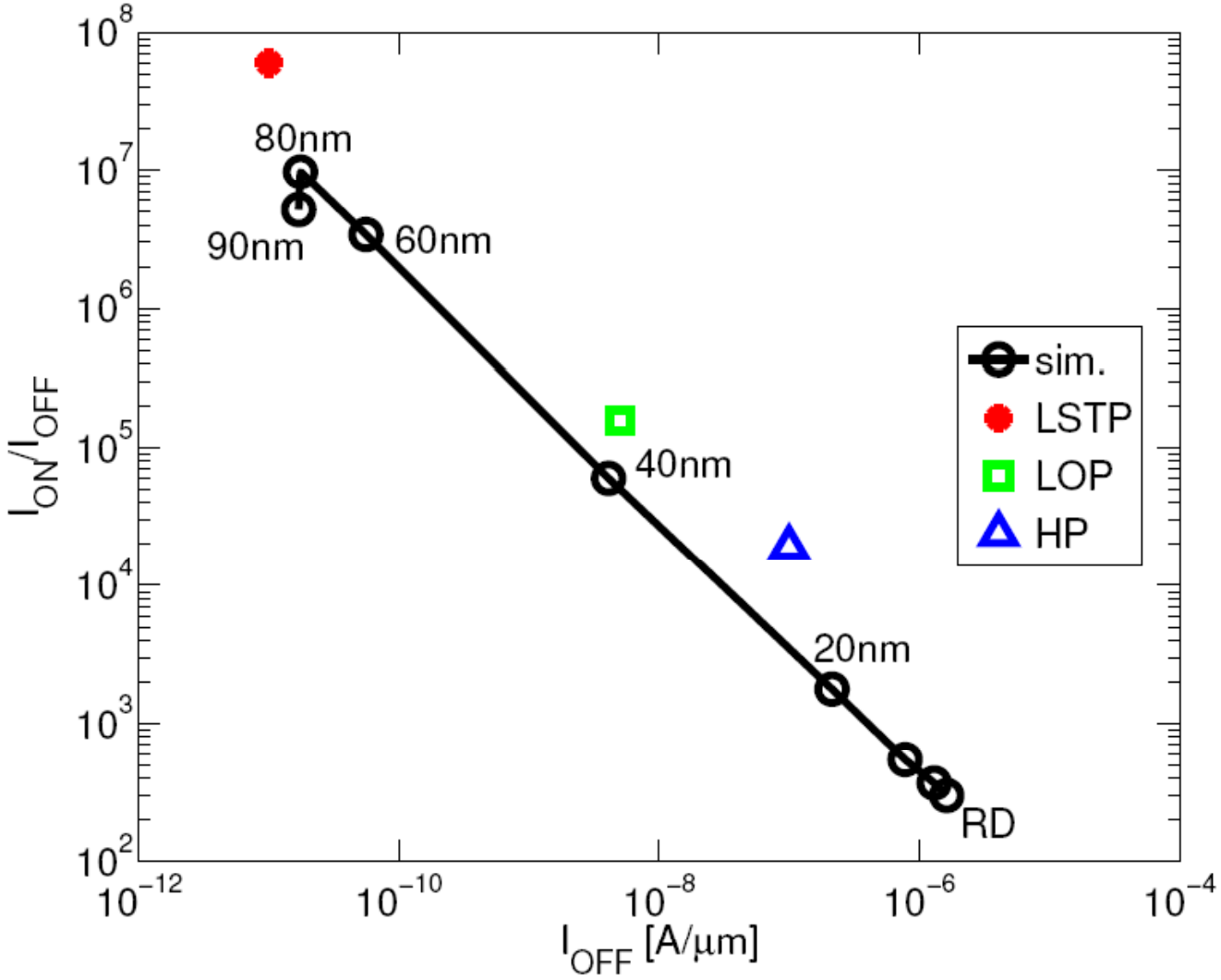
BONUS SLIDES

Summary of devices features

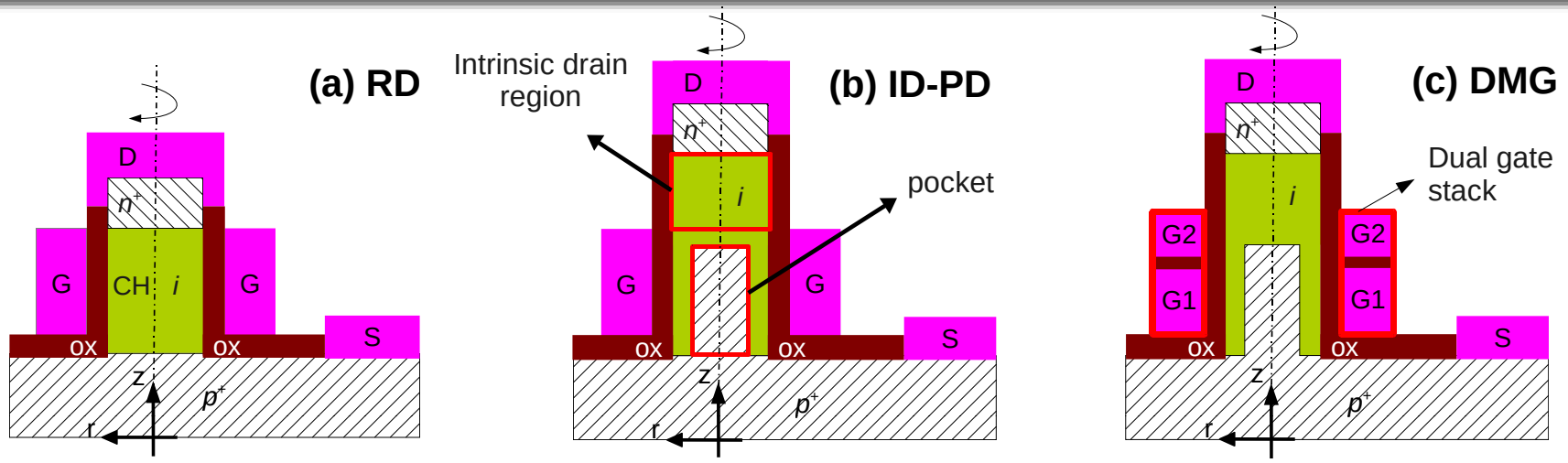


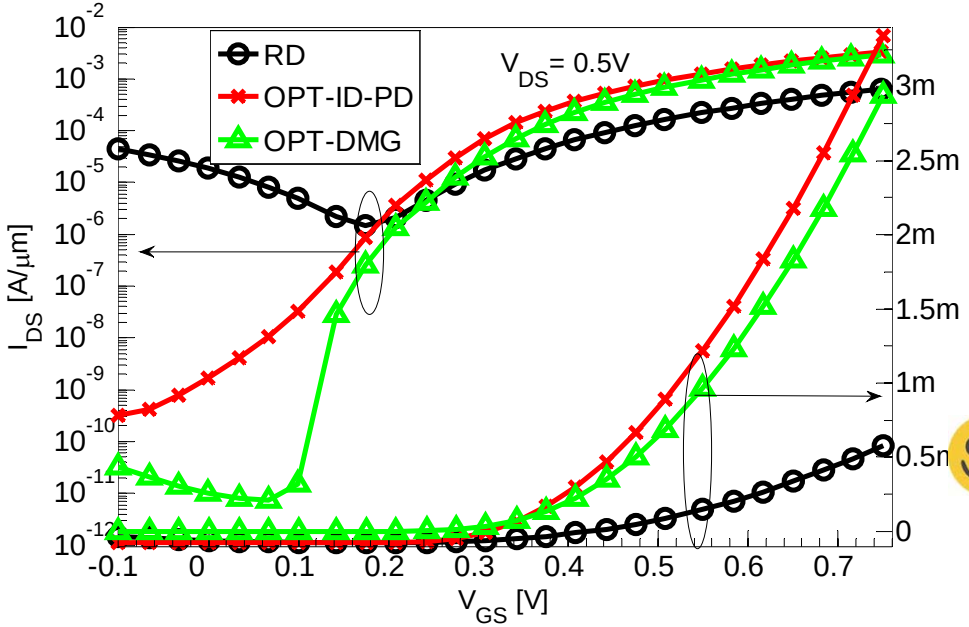
	RD	IPD	70nm-ID-RD	OPT-ID-PD
NW radius [nm]	10	10	10	10
CH length [nm]	40	40	40	40
S p^+-doping [cm^{-3}]	5×10^{19}	7×10^{19}	5×10^{19}	7×10^{19}
D n^+-doping [cm^{-3}]	5×10^{18}	5×10^{18}	5×10^{18}	5×10^{18}
t_{ox} [nm]	1.8	1.6	1.8	1.6
P length [nm]	-	35	-	35
P radius [nm]	-	6	-	6
P p^+-doping [cm^{-3}]	-	7×10^{19}	-	7×10^{19}
ID length [nm]	-	-	70	70

ID-RD: I_{ON}/I_{OFF} vs. I_{OFF} with varying ID length



The Dual-Metal-Gate (DMG) device





DMG-TFET, key features:

1. Further increasing of ID up to 100nm for lower I_{OFF}
2. Optimization of G2 length and WF

Avg. SS of about 42 mV/dec
point SS < 60 mV/dec over 5 I_{DS}-orders
min point SS of 7 mV/dec on 1 I_{DS}-order

Contact resistance: comparison with ITRS on I_{ON}

- ITRS: degradation of 37.5% is expected at year 2020 due to parasitic resistances

- LOP: 1.601 mA/μm – 37.5% ~ 1.001 mA/μm, still bigger than 0.784 mA/μm target
- HP: 1.904 mA/μm – 37.5 % ~ 1.190 mA/μm, still above 1mA/μm, as claimed in the paper.

→ To target HP, pocket length must be increased of about 50 nm to enhance I_{ON} of about 700 μA/μm.