Porous Si Dielectric Parameter Extraction for use in RF Passive Device Integration: Measurements and Simulations

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Outline

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4. Dielectric Characterization of porous Si
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Introduction

- Why RF circuits?
  - Wireless Communications
    - FM (100 MHz): 3 m
    - GSM (900 MHz): 33 cm
    - Wi-Fi (2.4 GHz): 12.5 cm
    - Q-band (33-50 GHz): 9-6 mm
    - W-band (75-110 GHz): 4-2.7 mm

- Why on-chip RF circuits?
  - Cost reduction.
  - Reduction of losses and parasitics due to wirebonds.
Standard CMOS silicon (1-10 Ω.cm) is
- a very lossy material ⇒ high RF losses in the substrate
- a high \( \varepsilon_r \) material (11.7) ⇒ e.g. high crosstalk

**This mainly affects:**

- Integration of RF passive devices (\( T \)lines, \textit{inductors}, \textit{filters} …)
- Integration of antennas

**Some examples ….**

1. Difficult to achieve high \( Z_c \) transmission lines
2. Difficult to achieve inductors that resonate at high frequencies
3. High energy loss in the surface waves inside the substrate
On-chip RF passives – Solutions for high performance

- On chip solutions under investigation
  - New topologies:
    > patterned metal shield below the devices e.g. Slow-wave CPW moderate-losses, CMOS processing, low-cost
  - Trap-rich HR-SOI
    > HR-Si with a trap-rich layer for use in SOI processes low-losses, SOI CMOS processing, expensive
  - **Porous Silicon**
    > local formation of porous Si on a bulk wafer, underneath the passive devices low-losses, compatible with batch Si processing, low-cost

...not applicable to all devices
What is Porous Silicon?

- **Formation:**
  > Electrochemical dissolution of Si in HF solution

Fabrication Parameters:
1. Si wafer Type
2. Si wafer Resistivity
3. Electrolytic Solution
4. Anodization Current

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ESSDERC 2013, Bucharest, 17.08.2013
Porous Silicon as an RF material

- Dielectric parameters of porous Si are highly dependent on Porosity, Structure, Morphology

  Tunability of $\varepsilon_r$ and $\tan\delta$

  $\Rightarrow$ Need for accurate and reliable parameter extraction for the specific material used

**TARGET:** To have a **reproducible** material with the desired and **well characterized** parameters which can be used in **RF simulation** tools resulting in good agreement between simulation and measurements
Dielectric Parameters of Porous Si

- Tunable $\varepsilon_r$
  - range: 2-9
  - (c-Si: 11.7 @ 25 °C)

- Low loss tangent
  - $\sim$0.02-0.05

- Stable dielectric parameters over T
  - T=20-170°C

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Increased porosity > reduced dielectric constant

The experimental values of $\varepsilon_r$ are in-between the values predicted by Vegard’s and Bruggeman’s models.

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Porous Silicon Characterization Method

- Dielectric Characterization
  1. Fabrication of the PSi layer
     \((p^+, \text{ porosity } 75\%, \ 200 \ \mu\text{m thick})\)
  2. Integration of a Coplanar Waveguide (CPW) on it
  3. S-parameters measurements
     \((1-40 \ \text{GHz})\)
  4. Conformal Mapping Method
     - Quasi-TEM mode
     - Valid until 400 GHz

Parameter Extraction

- Extraction of $\varepsilon_{r,PSi}$
  \[\varepsilon_{\text{eff}} = 1 + q_1 (\varepsilon_{r,\text{Si}} - 1) + q_2 (\varepsilon_{r,\text{PSi}} - \varepsilon_{r,\text{Si}}) + q_2 (\varepsilon_{r,\text{cap}} - \varepsilon_{r,\text{PSi}})\]  
  (eq. 1)
  where  \[q_j = \frac{1}{2} \left\{ \frac{K(k_j)}{K(k_0)} \right\}, \quad j = 1, 2, 3.\]

- Extraction of $\tan \delta_{PSi}$
  \[a_S = a_{T, PSi} - a_{T, \text{Simulations}}\]
  (eq. 2)
  \[= \frac{\pi f}{c \cdot \sqrt{\varepsilon_{\text{eff}}}} \cdot \left\{ \left( q_1 - q_2 \right) \varepsilon_{r,\text{Si}}' \cdot \tan \delta_{\text{Si}} \right\} + \left( q_2 - q_3 \right) \varepsilon_{r,\text{PSi}}' \cdot \tan \delta_{\text{PSi}} + q_3 \varepsilon_{r,\text{cap}}' \cdot \tan \delta_{\text{cap}}\]

New Algorithm!

- CPW TL S-parameter measurements
- Extract $\varepsilon_{r,PSi}$ according to CMM (eq. 1)
- Simulate the CPW TL on substrate with $\varepsilon_r = \varepsilon_{r,PSi}$, $\tan \delta = 0$
- Extract $\tan \delta_{PSi}$ according to eq. 2
- PSi dielectric properties for the designer

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Reliability of the Extraction Method

1. We have performed the extraction of the dielectric parameters on 6 different samples with 145 Ω CPW integrated on them
2. We have used the extracted values to simulate the same 6 devices using HFSS
3. We compare the simulations to the measurements

$$\Rightarrow$$ The maximum average deviation between measurement and simulation was:

- 1.2 dB for $S_{11}$
- 0.5 dB for $S_{12}$

<table>
<thead>
<tr>
<th>CPW Device</th>
<th>$Z_c$ [Ω]</th>
<th>$E_{11}$ [dB]</th>
<th>$E_{12}$ [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPW1</td>
<td>145</td>
<td>1.2</td>
<td>0.4</td>
</tr>
<tr>
<td>CPW2</td>
<td>145</td>
<td>1.1</td>
<td>0.5</td>
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<tr>
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</tr>
<tr>
<td>CPW5</td>
<td>145</td>
<td>0.5</td>
<td>0.3</td>
</tr>
<tr>
<td>CPW6</td>
<td>145</td>
<td>0.5</td>
<td>0.2</td>
</tr>
</tbody>
</table>
We extract the values of $\varepsilon_r$ and $\tan\delta$ of a PSi layer

We feed these values into HFSS to simulate the performance of 50, 100, 145Ω CPW Tlines

We compare the simulations to the measurements of devices fabricated on PSi
We extract the values of $\varepsilon_r$ and $\tan\delta$ of a PSi layer using a CPW.

We feed these values into HFSS to simulate the performance of inductors:
- 2.5 turns – 3.2 nH
- 3.5 turns – 6.1 nH

We compare the simulations to the measurements of inductors fabricated on PSi having the used parameters.
In order to demonstrate the effectiveness of porous Si as an RF substrate, we compare it with different state-of-the-art substrates.
Comparison of Different Substrates

CPWs on four different substrates
Comparison of performance

Values for PSi @ 40 GHz
\[ \alpha = 0.2 \text{ dB/mm} \]
\[ Q = 25 \]
\[ Z_c = 90\Omega \]
\[ \varepsilon_{eff} = 1.5 \]

Comparable to quartz substrate! (off-chip)

Conclusions

A method to accurately extract the dielectric parameters of porous Si has been developed. Its validity has been proven.

Very good agreement between simulation and measurement for TLines and inductors has been obtained.

A comparison between porous Si and other state-of-the-art substrates for RF was made. The superiority of porous Si has been shown.

The developed method for RF extraction opens the possibility of using commercial simulation programs to accurately design RF devices on porous Si.
Thank you for your attention!

This work was supported by the EU Network of Excellence NANOFUNCTION through the EU 7th FP for Research under Contract 25375

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