An Experimental Study of Integrated DMOS Transistors with Increased Energy Capability

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Outline

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Motivation

Proposed Optimization Approaches

- Basic Idea
- Requirements
- Approaches

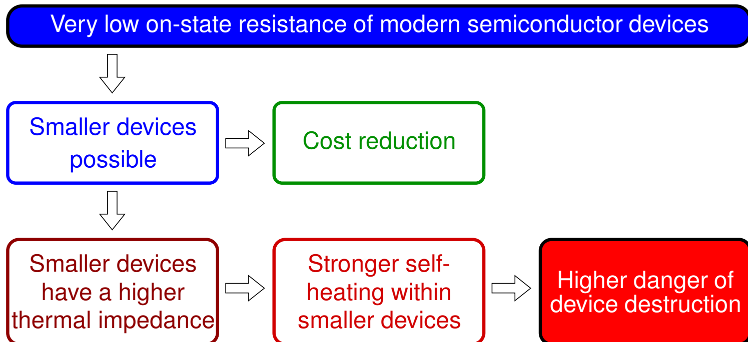
Application to Test Structures

- Simulations
- Measurements

Application to a More Complex Structure

Conclusion

Motivation



- ➔ **Size reduction limited by thermal constraints,** $R_{DS,on}$ better than actually required
- ➔ Trade-off between **size** and **maximum device temperature**

Focus: Reduce maximum device temperature

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Temperature Distribution within a Power DMOS

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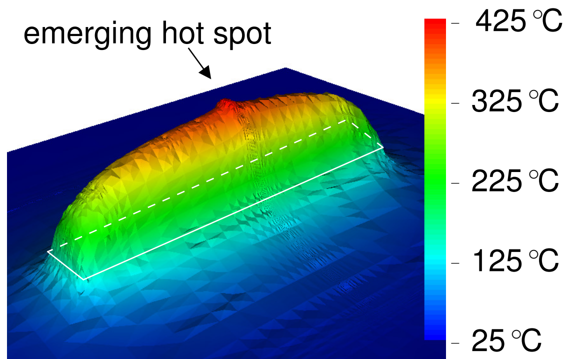


Peak temperatures in the device center, outer areas cooler

Main question: How to reshape the temperature distribution?

Basic Idea

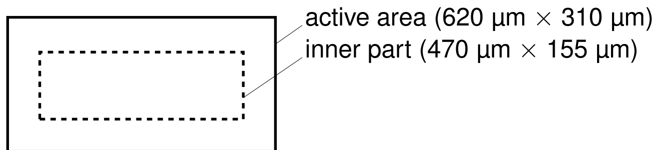
Idea: Temperature and power dissipation are closely related
→ **Selectively change the power dissipation density**

- Reduce in the hotter DMOS areas
- Increase in the cooler DMOS areas

→ **Separate DMOS regions** with **different characteristics** needed

Considering the temperature distribution (see above): Division of the DMOS into an **inner** and an **outer part**

Possible approach:



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Requirements

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Absolute Requirements:

- **Only layout changes**, no technology modification, no changes of the fabrication process
- No effect on the **breakdown voltage**
- **Feasible for industrial designs**

Optional Requirements:

- No impact on the **on-state resistance**
- No changes of the **external circuitry**

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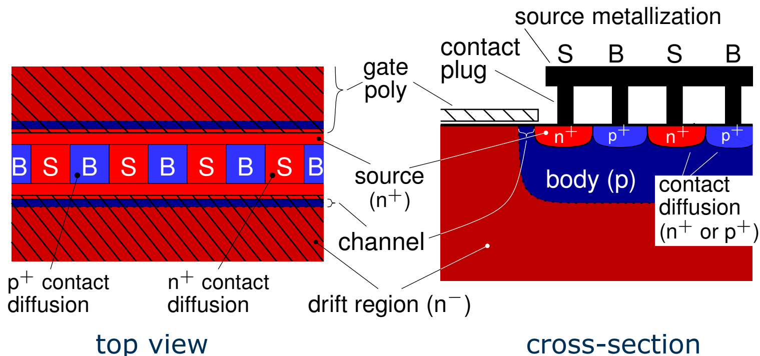
Structure of the investigated DMOS

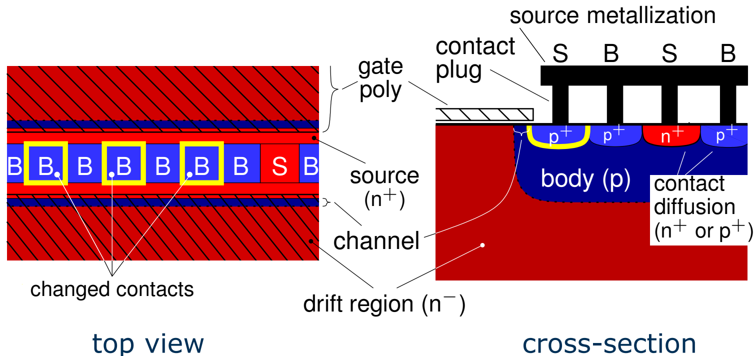


How to reduce the power dissipation density in this area?

→ Reduction of current density

1.) Reduced Source Contact Density

Source contacts in the hottest areas **selectively replaced by body contacts**



Less number of source contacts → less current flow

2.) Separated Gates

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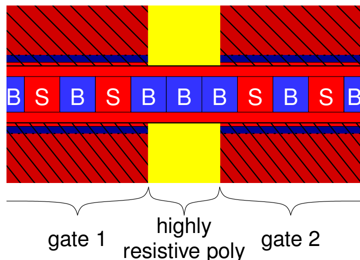
Division of the device into **two separately controllable gate regions**

Separation of the regions by a **highly resistive poly area**



Gate in the hot areas can be turned off if needed.

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Test Structure

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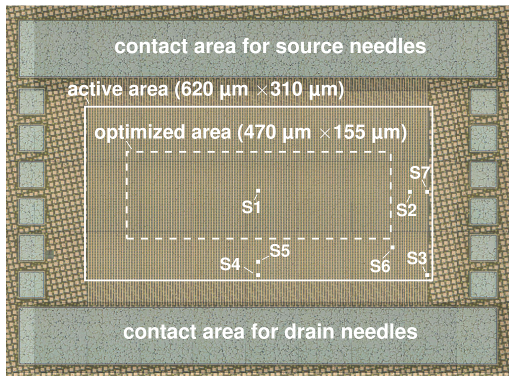


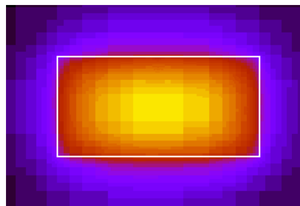
Fabricated in a **state-of-the-art 0.18 µm BCD** technology

Measured **on-wafer**

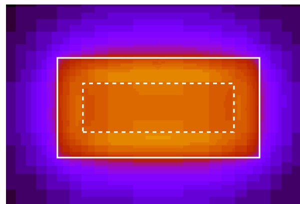
Embedded **temperature sensors** for accurate measurement

Simulation – Reduced Src. Cnt. Density

reference device



reduced src. cnt. density



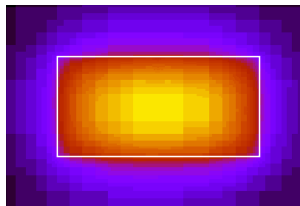
Parameters:
$t_{\mathrm{pul}} = 1\mathrm{ms}, V_{\mathrm{DS}} = 20\mathrm{V}, I_{\mathrm{D}} = 1.67\mathrm{A}$

Reduced source contact density

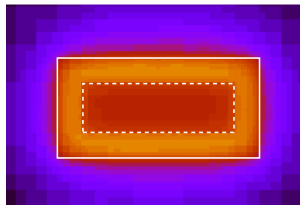
- → **Reduced dissipated power** in the center area
- → **Peak temperature** reduced from **350°C** to **300°C** (corresponds to **20% area reduction**)
- → **Temperature distribution more uniform**

Simulation – Inner Gate Turned Off

reference device



inner gate off



Parameters:
$t_{\mathrm{pul}} = 1\mathrm{ms}, V_{\mathrm{DS}} = 20\mathrm{V}, I_{\mathrm{D}} = 1.67\mathrm{A}$

Inner gate turned off

- → **No power dissipation** in the center area
- → **Peak temperature** reduced from **350°C** to **300°C**
- → **Inner area cooler** compared to the reduced source density device

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Measurement Results

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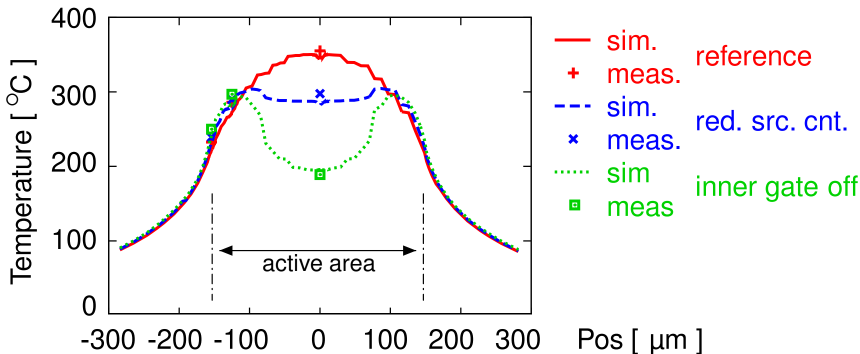
Temperature measurement and **simulation** in comparison



→ **Temperature reduction** clearly visible

→ Good **agreement** of measurement and simulation

Energy Capability – Reduced Src. Cnt. Density

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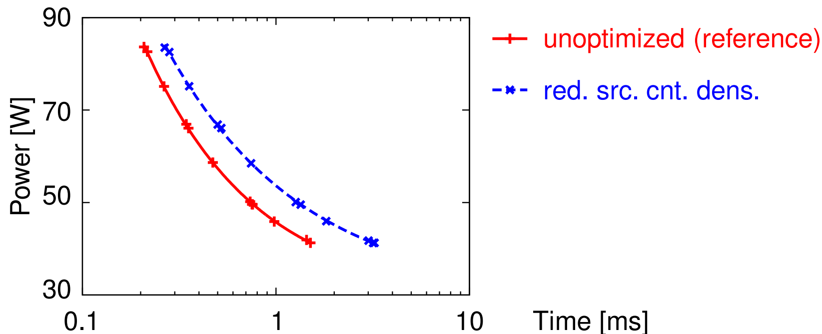
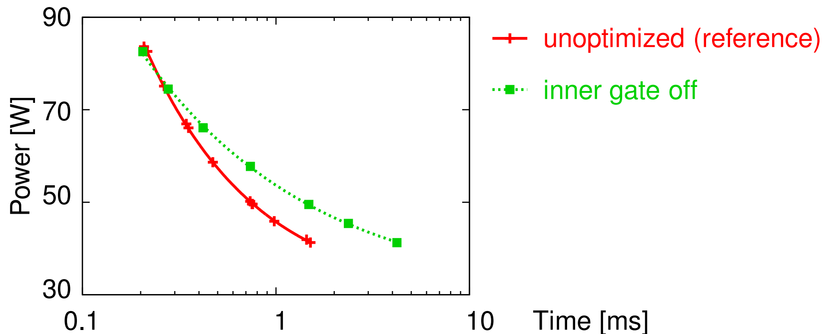
Time until device failure (measured at $V_{DS} = 20V..50V, I_D = 1.67A$)



➔ **Significant increase of energy capability** especially at moderate power pulses due to lower peak temperatures

Energy Capability – Inner Gate Turned Off



→ At **low power pulses even better** than the reduced source contact density device

But: **Worse** than the reference device at **high power pulses**:

- Only outer area is turned on → **very high power density**
- Much **heat** generated in a very short time

Electrical Parameters

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On-state resistance $R_{DS,on}$

- **Reference** device (not optimized): **0.3 Ω**
- **Reduced source contact density** device: **0.33 Ω**
  ➔ $R_{DS,on}$ only **slightly increased**
- **Separated gate** device
  - **Inner gate turned off**: **0.48 Ω**
    ➔ High $R_{DS,on}$, but **only in case of high power dissipation**
  - **Inner gate turned on** (if V_{DS} is low): **0.3 Ω**
    ➔ **No $R_{DS,on}$ increase**

Breakdown voltage not affected by any approach

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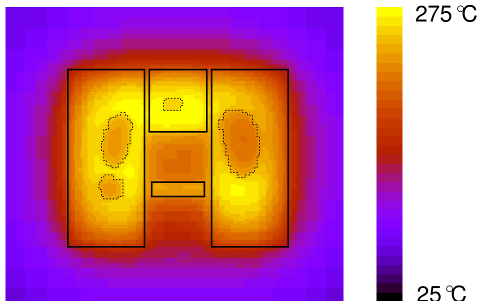
Thermal Behavior

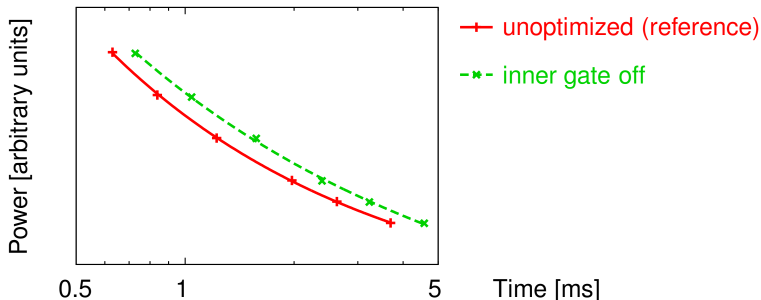


Inner gates turned off in the marked areas

Thermal behavior already better due to inactive center region

Further 7% peak temperature reduction (10% area reduction) by our approach

Energy Capability



25% energy capability improvement by our approach

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Two **easily applicable** approaches to improve the energy capability of a LDMOS **only by layout modification** have been presented.

Both approaches allow a **significant reduction of the peak device temperature** or of the **device area**.

Acceptable $\boldsymbol{R_{\mathrm{DS,on}}}$ increase, no effect on **breakdown voltage**

Approaches **easy to implement** in existing technologies

Easy applicable to **industrial designs**

Ongoing work: More optimized structures, **automated layout generation**

Thank you very much
for your attention.

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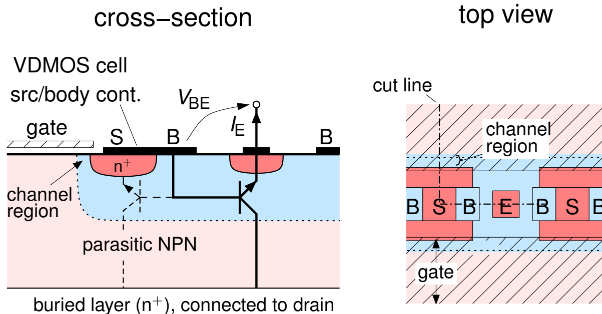
We start with a (vertical) DMOS.

Disconnect one n^+ region from the DMOS source
Only layout changes required for that



→ We **obtain a bipolar NPN transistor** (like the parasitic NPN)